

**No. 15-1091**

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**United States Court of Appeals  
for the Federal Circuit**

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**MCM PORTFOLIO LLC,  
APPELLANT,**

**v.**

**HEWLETT-PACKARD COMPANY,  
APPELLEE.**

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**APPEAL FROM PATENT AND TRADEMARK OFFICE –  
PATENT TRIAL AND APPEAL BOARD IN NO. IPR2013-00217**

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**MOTION TO STAY REISSUE BY APPELLANT  
MCM PORTFOLIO LLC**

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*Attorneys for Appellant*

Dated: February 10, 2015

**CERTIFICATE OF INTEREST**

1. The full name of every party represented by me:

**MCM Portfolio LLC**

2. Other real parties in interest represented by me:

**None**

3. All parent corporations and any publicly held companies that own 10 percent or more of the stock of the party or amicus curiae represented by me are:

**None**

4. The names of all the firms or lawyers that appeared for MCM Portfolio LLC in the *Inter Partes* Review and who are expected to appear in this case:

**Edward P. Heller III and Susan L. Anhalt**

/s/ Edward P Heller III

Edward P Heller III

Dated: February 10, 2015

## **I. RELIEF REQUESTED**

An order directing the Director to withdraw the action dated January 12, 2015, and to place the further prosecution of reissue patent application number 12/351/691 on hold, pending the mandate of this court in No. 15-1091, MCM Portfolio LLC v. Hewlett-Packard Company, unless otherwise ordered by this court.

## **II. CONSENT OF PARTIES**

MCM has requested consent from both parties to the relief requested by present motion. The Director indicates that she will oppose the motion. Hewlett-Packard has indicated that it does not consent.

## **III. GROUNDS**

### **A. Procedural Background**

On September 12, 2014, in paper number 32 of IPR number IPR2013-00217, A1-A4 (Lifting Stay), and prior to the time expired for MCM to file a notice of appeal of the final written decision, the Board, without consulting with MCM and on its own motion, lifted the stay it had imposed on the prosecution of reissue application 12/351/691, a

reissue application for US patent number 7,162,549 B2, the patent under consideration in the present appeal, that it had entered on May 10, 2013 at the request of Hewlett-Packard, and without opposition by MCM. A1-A4 (Stay)

MCM filed its notice of appeal with respect to on October 1, 2014. A8.

On November 5, 2014, the Director reopened prosecution of the aforementioned “691 reissue application. A46. On November 14, 2014, MCM cancelled all disallowed claims. A49-A71. All remaining claims, including claims 7, 11, 19 and 21, were previously allowed. Claims 7, 11, 19 and 21, as previously allowed, were allowed in an amended state from US ‘549. *Ibid.*

In an Action dated January 12, 2015, the examiner rejected all pending claims but two, claims 20 and 22, which he allowed. A72-A89. Claims 7, 11, 19 and 21 were rejected over Kobayashi in view of Kikuchi, the same two references that form the basis of the Board’s final written decision in the above-referenced IPR. *Ibid.* The examiner did not reject the claims over any other prior art cited in the HP

petition filed in the above-referenced IPR. In the office action, the examiner stated,

2. Prosecution on the merits of this application is reopened on claims 7-16, 19-22, 37-41 and 43-50. Consideration is made in light of the final written decision by the PTAB on 8/6/2014 for US Pat. No. 7,162,549, in which this instant application is a reissue thereof, and the Information Disclosure Statements submitted on the 4/4/2013.

*Ibid.*

The Action gave MCM until April 15, to respond, otherwise the application will be regarded as abandoned. 35 U.S.C. 133. While MCM, with the payment of substantial fees, may extend the time for response another three months, MCM cannot extend the time to respond beyond six months. *Id.* That date is July 12, 2015.

On January 29, MCM phoned the Director's counsel, Scott Weidenfeller, and requested that the reissue application be again placed on hold for the very same reasons it was placed on hold by the Board in its May 10, 2013 order. On, February 3, MCM followed up. On Friday, February 6, 2013, Mr. Weidenfeller responded that the

Director would not withdraw the outstanding office action of January 12, 2013 and again place the reissue application on hold.

**B. Argument**

In its May 10, 2013 order, the Board stated:

Conducting the examination of the '691 reissue application concurrently with the instant proceeding would duplicate efforts within the Office and could potentially result in inconsistencies between the proceedings. Notably, the patentability of claims 7, 11, 19, and 21 of the '549 patent is being determined in both proceedings. ... If the prosecution is reopened, Patent Owner could amend the claims in the reissue application and change the scope of the challenged claims while the Board is conducting its review (should a review be instituted).

...

Any Board decision on whether to institute a review or final written decision with respect to the patentability of the challenged claims may simplify the issues in the reissue application as well.

A2-A3. Notably, the same considerations apply today with respect to the reissue application and the present appeal as applied then between the reissue application and the IPR.

Moreover, an examiner is not free to disregard a final decision of the Board to which the January 12 Action directly refers, rendering anything that MCM might say substantively unavailing until the Board's decision is either reversed or vacated by this court. Forcing MCM to

proceed with the prosecution of the reissue under the present circumstances denies MCM due process because it forces MCM to file an expensive, but unavailing reply, to pay money for late fees, appeals or the like, or to have its application go abandoned.

The Director is a party to this appeal and subject to the jurisdiction of this court. The relief requested is within the discretion of the Director and her denial of the present relief is inconsistent with the previous stay order of the Board. It is further inconsistent with fundamental notions of due process. There does not appear to be any justifiable basis not to withdraw the outstanding office action of January 12, 2015, and to once again place the reissue application on hold.

The present relief by this court is authorized by 5 U.S.C. 705, which reads

§ 705. Relief pending review

When an agency finds that justice so requires, it may postpone the effective date of action taken by it, pending judicial review. On such conditions as may be required and to the extent necessary to prevent irreparable injury, the reviewing court, including the court to which a case may be taken on appeal from or on application for certiorari or other writ to a reviewing court, may issue all necessary and appropriate process to postpone the effective date of an agency

action or to preserve status or rights pending conclusion of the review proceedings.

As discussed above, an examiner cannot overturn the Board. Requiring MCM to respond substantively to the office action imposes harm on MCM due to the expense of responding to the outstanding action. Regardless of the response, the examiner will enter a final action, forcing another appeal to the same Board who has already decided the issue presented, but at significant expense both in fees and manpower both to MCM and the Director. If MCM chooses to not expend these resources to accomplish nothing, its reissue application will go abandoned.

Alternatively, if MCM choses to cancel all but the allowed claims (without prejudice) in order to “buy time,” the Direct may issue a notice of allowance giving MCM just three months to pay the issue fee. When such a reissue patent issues, the ‘549 patent will be surrendered, ending the res and the jurisdiction of this court to decide the merits, and causing MCM substantial damage because of the loss of its claims without having the present appeal decided.

Regardless of what MCM does, it has no recourse but to spend money to buy time, or to file unavailing responses to office actions, or to surrender the '549 patent. MCM is in a no-win situation, and justice demands a stay that will cost the Director nothing, and which, with respect to HP, is consistent with HP's prior request for a stay in the first instance.

Respectfully submitted,

/s/ Edward P. Heller III

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Dated: February 10, 2015

# ADDENDUM

Paper No.	Date	Document Description	Pages Included	Pages
8	5/10/13	ORDER Staying Concurrent Examination of Reissue Application - Case IPR2013-00217	All	A1-A4
32	9/12/14	ORDER Lifting Stay of Concurrent Reissue Application - Case IPR2013-00217	All	A5-A7
N/A	10/1/14	Notice of Appeal to the Federal Circuit	All	A8-A45
N/A	11/5/14	Notice of Reopening of Prosecution in Accordance with PTAB Order Lifting Stay	All	A46-A48
N/A	11/14/14	§ 41.33 AMENDMENT Filed for 12/351,691	All	A49-A71
N/A	1/12/15	Non-Final Office Action for 12/351,691	All	A72-A89

[Trials@uspto.gov](mailto:Trials@uspto.gov)

571-272-7822

Paper 8

Entered: May 10, 2013

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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HEWLETT-PACKARD COMPANY,  
Petitioner,

v.

MCM PORTFOLIO LLC.  
Patent Owner.

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Case IPR2013-00217 (JYC)  
Patent 7,162,549

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Before SCOTT R. BOALICK, KARL D. EASTHOM, and JONI Y. CHANG,  
*Administrative Patent Judges.*

CHANG, *Administrative Patent Judge.*

ORDER  
Staying Concurrent Examination of Reissue Application  
*37 C.F.R. § 42.122(a)*

Case IPR2013-00217

Patent 7,162,549

On May 9, 2013, a telephone conference call was held between respective counsel for the parties and Judges Boalick, Easthom, and Chang. During the conference call, counsel for Petitioner requested that the examination of the reissue application, U.S. Application No. 12/351,691 (“the ’691 reissue application”) be stayed. Patent Owner did not oppose the request. For reasons discussed below, Petitioner’s request to stay the concurrent examination of the ’691 reissue application is *granted*.

Section 315(d) of title 35 of United States Code, as amended by the America Invents Act (AIA), provides:

Notwithstanding sections 135(a), 251, and 252, and chapter 30, during the pendency of an inter partes review, if another proceeding or matter involving the patent is before the Office, the Director may determine the manner in which the inter partes review or other proceeding or matter may proceed, including providing for stay, transfer, consolidation, or termination of any such matter or proceeding.

The petition for *inter partes* review of Patent 7,162,549 (“the ’549 patent”) was filed on March 27, 2013. The petition challenges the patentability of claims 7, 11, 19, and 21 of the ’549 patent. The co-pending ’691 reissue application also involves the ’549 patent.

Conducting the examination of the ’691 reissue application concurrently with the instant proceeding would duplicate efforts within the Office and could potentially result in inconsistencies between the proceedings. Notably, the patentability of claims 7, 11, 19, and 21 of the ’549 patent is being determined in both proceedings. A notice of appeal was filed on May 1, 2013 in the ’691 reissue application. The Board was informed by the parties that while the challenged claims are not rejected by the Examiner in the ’691 reissue application, some of the prior art references relied upon in the *inter partes* review petition have not been

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Patent 7,162,549

considered by the Examiner. If the prosecution is reopened, Patent Owner could amend the claims in the reissue application and change the scope of the challenged claims while the Board is conducting its review (should a review be instituted).

In addition, staying the examination of the '691 reissue application would not impact any statutory time period for the Examining Corps, as the prosecution is closed and the time period for filing an appeal brief is a regulatory time period (*see* 37 C.F.R. § 41.37(a)).

Moreover, the Board is required to determine whether to institute an *inter partes* review within three months after receiving a preliminary response from Patent Owner, or the date on which such a response is due. *See* 35 U.S.C. § 314(b), as amended by the AIA. The final determination of any review instituted will normally be issued no later than one year from institution. *See* 35 U.S.C. § 316(a)(11), as amended by the AIA; 37 C.F.R. § 42.100(c). Any Board decision on whether to institute a review or final written decision with respect to the patentability of the challenged claims may simplify the issues in the reissue application as well.

Based upon the facts presented in the instant proceeding and in the '691 reissue application, the Board exercises its discretion under 35 U.S.C. § 315(d), as amended by the AIA, and 37 C.F.R. § 42.122(a), and orders that examination of the '691 reissue application be stayed pending the termination or completion of the instant proceeding.

Case IPR2013-00217

Patent 7,162,549

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Paper 32  
Entered: September 12, 2014

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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HEWLETT-PACKARD COMPANY,  
Petitioner,

v.

MCM PORTFOLIO, LLC,  
Patent Owner.

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Case IPR2013-00217  
Patent 7,162,549 B2

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Before JONI Y. CHANG, GLENN J. PERRY, and JENNIFER S. BISK,  
*Administrative Patent Judges.*

CHANG, *Administrative Patent Judge.*

ORDER  
Lifting Stay of Concurrent Reissue Application  
37 C.F.R. § 42.122(a)

Case IPR2013-00217  
Patent 7,162,549 B2

On March 27, 2013, Petitioner Hewlett-Packard Company (“HP”) filed a Petition (Paper 2) to institute an *inter partes* review of claims 7, 11, 19, and 21 of U.S. Patent No. 7,162,549 B2 (Ex. 1001, “the ’549 patent”).

HP requested the concurrent examination of the reissue application, U.S. Application No. 12/351,691 (“the ’691 reissue application”) be stayed. Paper 8. Patent Owner MCM Portfolio, LLC (“MCM”) did not oppose. *Id.* Upon consideration of the facts presented, we exercised our discretion under 35 U.S.C. § 315(d) and 37 C.F.R. § 42.122(a), and entered an Order staying the concurrent examination of the ’691 reissue application. *Id.*

On August 6, 2014, we entered a Final Written Decision under 35 U.S.C. § 318(a), determining claims 7, 11, 19, and 21 of the ’549 patent to be unpatentable. Paper 31. Under the present circumstances, we are persuaded that the stay should be lifted before the time for any appeal has expired and any appeal has terminated.

In consideration of the foregoing, it is hereby:

ORDERED that the stay of the concurrent examination of the ’691 reissue application is lifted.

Case IPR2013-00217  
Patent 7,162,549 B2

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UNITED STATES PATENT AND TRADEMARK OFFICE  

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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HEWLETT-PACKARD COMPANY,  
Petitioner

v.

MCM PORTFOLIO LLC,  
Patent Owner

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Case No. IPR2013-00217  
Patent No. 7,162,549

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Notice of Appeal to the Federal Circuit

To: Office of the General Counsel  
U.S. Patent and Trademark Office  
P.O. Box 1450  
Alexandria, VA 22313-1450

And to

Mail Stop 8  
Office of the Solicitor  
U.S. Patent and Trademark Office  
PO Box 1450  
Alexandria, VA 22313-1450

Patent Owner hereby provides notice of appeal to the US Court of Appeals for the Federal Circuit under 35 USC §§ 141 and 142 from the final written decision of the patent trial and appeal board dated August 8, 2014, and from the institution decision dated September 10, 2013, rehearing denied October 10, 2013.

Pursuant to rule 90.2(b)(3)(ii) the expected issues on appeal will include

1. Whether the decision of the Federal Circuit in *Patlex* that a patent is a public right was in error such that a patent owner does not have a constitutionally protected rights to both a trial in an Art. III court, and to a Jury to determine the validity of its patent.
2. Whether HP presented a *prima facie* case of obviousness pursuant to its statutory burden of proof when it failed to even allege, let alone prove that a claimed controller chip having all the required functionality of independent claims 7 and 11.
3. Whether the PTAB's equitable balancing test standard for

determining 315(b) privity is inconsistent with Taylor v. Sturgell, thereby impermissibly denying patent owner the benefits of 315(b).

Patent owner has electronically filed this notice with the Patent Trial and Appeal Board.

Simultaneously herewith, patent owner is providing the Federal Circuit three copies of the present Notice of Appeal together with a \$500 fee pursuant to its rule 52.

All copies include a copy of the final written decision, the institution decision and the rehearing decision.



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## CERTIFICATE OF SERVICE

The undersigned hereby confirms that the foregoing Notice of Appeal was served on October 1, 2014, via email, upon [HP549IPR@kenyon.com](mailto:HP549IPR@kenyon.com); and upon counsel record, Robert L. Hails, Jr ([rhails@Kenyon.com](mailto:rhails@Kenyon.com)) and T. Cy Walker ([cwalker@Kenyon.com](mailto:cwalker@Kenyon.com)).



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/Edward P. Heller III/  
Edward P. Heller III,  
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Paper 31  
Entered: August 6, 2014

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

---

HEWLETT-PACKARD COMPANY,  
Petitioner,

v.

MCM PORTFOLIO, LLC,  
Patent Owner.

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Case IPR2013-00217  
Patent 7,162,549

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Before JONI Y. CHANG, GLENN J. PERRY, and JENNIFER S. BISK,  
*Administrative Patent Judges.*

BISK, *Administrative Patent Judge.*

FINAL WRITTEN DECISION  
*35 U.S.C. § 318(a) and 37 C.F.R. § 42.73*

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Patent 7,162,549

## I. INTRODUCTION

### A. Background

Petitioner Hewlett-Packard Company (“HP”) filed a Petition (Paper 2, “Pet.”) to institute an *inter partes* review of claims 7, 11, 19, and 21 (the “challenged claims”) of U.S. Patent No. 7,162,549 (Exhibit 1001, “the ’549 patent”) under 35 U.S.C. §§ 311-319. Patent Owner MCM Portfolio, LLC (“MCM”) filed a Preliminary Response. Paper 9. On September 10, 2013, we instituted trial (Paper 10; “Decision”), concluding that Petitioner had demonstrated a reasonable likelihood of showing that the challenged claims are unpatentable under 35 U.S.C. § 103 over U.S. Patent No. 6,199,122 (Ex. 1005) (“Kobayashi”) combined with WO 98/03915 (Ex. 1007) (“Kikuchi”). Decision 3, 16.

We have jurisdiction under 35 U.S.C. § 6(c). This final written decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73.

Petitioner has shown by a preponderance of evidence that claims 7, 11, 19, and 21 are *unpatentable*.

### B. Related Proceedings

The parties list several cases pending in the Eastern District of Texas that would affect or be affected by the decision in this proceeding, including *Technology Properties Limited, LLC v. Hewlett-Packard Co.*, No. 6:12-cv-208 (E.D. Tex. Mar. 28, 2012), in which the ’549 patent is asserted against Petitioner. *See* Pet. 1; Paper 6, 1. On February 11, 2014, after a finding of No Violation of Section 337 in a concurrent proceeding at the International Trade Commission (No. 337-TA-841), a stay of the 6:12-cv-208 case was lifted and it was consolidated with *Technology Properties Limited, LLC v. Cannon, Inc. et al.*, No. 6:12-cv-202 (E.D. Tex. Mar. 28, 2012). A

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Patent 7,162,549

Markman Hearing is currently scheduled in that case for October 8, 2014.

*Technology Properties Limited, LLC v. Cannon, Inc. et al.*, No. 6:12-cv-202 (E.D. Tex. Mar. 14, 2014).

In addition, the '549 patent is the subject of a pending reissue proceeding, US Application 12/351,691. We ordered a stay of that examination pending the termination or completion of this proceeding.

Paper 8.

*C. The '549 Patent*

The '549 patent relates to controllers for flash-memory cards. Ex. 1001, 1:21-22. As described in the “Background of the Invention,” at the time of the invention, removable flash-memory cards were commonly used with digital cameras to allow for convenient transfer of images from a camera to a personal computer. *Id.* at 1:26-56. These prior art flash-memory cards were available in several formats, including CompactFlash, SmartMedia, MultiMediaCard (MMC), Secure Digital Card (SD), and Memory Stick card. *Id.* at 2:28-55. Each of the card formats required a different interface adapter to work with a personal computer. *Id.* at 3:9-25.

The Specification describes a need for a flash-memory card reader that accepts flash-memory cards of several different formats using a universal adapter. *Id.* at 3:52-63. In response to this need, the '549 patent describes various improvements to flash-memory card readers, including by determining whether a particular flash-memory card includes a controller and, if not, performing operations to manage error correction for the flash-memory card. *Id.* at 3:24-65.

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Patent 7,162,549

*D. Illustrative Claim*

Claim 7, reproduced below, is illustrative of the claimed subject matter:

7. A method comprising:

using a controller chip to interface a flash storage system with or without a controller to a computing device, the controller chip comprising a flash adapter, wherein the flash storage system comprises a flash section and at least a medium ID;

determining whether the flash storage system includes a controller for error correction; and

in an event where the flash storage system does not have a controller for error correction, using firmware in the flash adapter to perform operations to manage error correction of the flash section, including bad block mapping of the flash section in the flash storage system that is coupled to the flash adapter section.

II. ANALYSIS

*A. Seventh Amendment*

As a preliminary matter, MCM argues that *inter partes* review proceedings violate the Seventh Amendment. PO Resp. 2-13. The U.S. Court of Appeals for the Federal Circuit, however, has previously rejected this argument in the context of reexaminations. *Patlex Corp. v. Mossinghoff*, 758 F.2d 594, 603-05 (Fed. Cir. 1985) (holding that even when applied retroactively, the reexamination statute does not violate the jury trial guarantee of the Seventh Amendment); *see also Joy Techs., Inc. v. Manbeck*, 959 F.2d 226, 228-29 (Fed. Cir. 1992) (affirming the holding in *Patlex*), *other grounds superseded by statute*, 35 U.S.C. § 145, *as recognized in In re Teles AG Informationstechnologien*, 747 F.3d 1357 (Fed. Cir. 2014). *Inter partes* review proceedings continue the basic functions of the reexamination proceedings at issue in *Patlex*—authorizing the Office to reexamine the

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Patent 7,162,549

validity of an issued patent and to cancel any claims the Office concludes should not have been issued. Patent Owner does not identify any constitutionally-significant distinction between reexamination proceedings and *inter partes* review proceedings. Thus, for the reasons articulated in *Patlex*, we conclude that *inter partes* reviews, like reexaminations, comply with the Seventh Amendment.

### *B. Claim Construction*

We construe all terms, whether or not expressly discussed here, using the broadest reasonable construction in light of the '549 patent specification. 37 C.F.R. § 42.100(b). For the purposes of the decision to institute we expressly construed the following terms: (1) “flash adapter” and “flash adapter section” as “a section of the controller chip that enables communication with the flash storage system” and (2) “bad block mapping” as a type of error correction. Decision 5-6. In the post-institution briefs, the parties do not dispute these constructions. *See* Paper 23 (“PO Resp.”); Paper 24 (“Reply”). For purposes of this decision, we continue to apply these constructions.

### *C. Overview of Kobayashi*

Kobayashi describes a memory device for a computer with a converter that converts serial commands of the computer to parallel commands that are then used to control a storage medium (which can be a flash-memory card). Ex. 1005, 2:55-64, 3:63-65. This configuration is shown in Figure 1, which is reproduced below.

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Patent 7,162,549

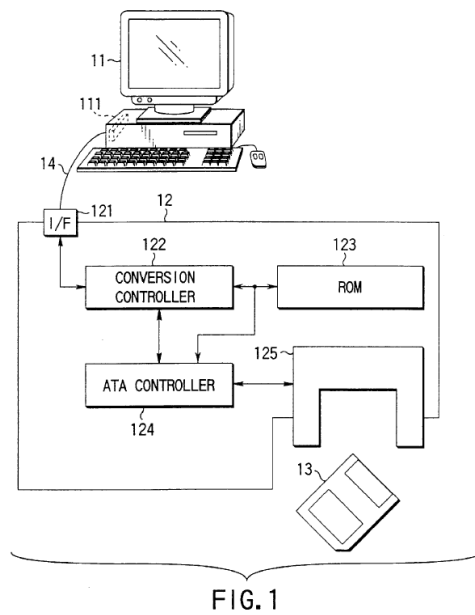
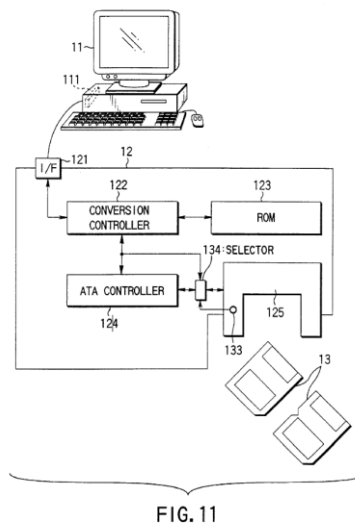


Figure 1 is a block diagram of computer 11 with reader/writer 12 and flash-memory card 13. *Id.* at 5:54-58. The reader/writer includes conversion controller 122, ATA controller 124, and a connector 125 for reading a flash-memory card 13. *Id.* at 6:5-9.

One of the several embodiments described by Kobayashi is shown in Figure 11, reproduced below.



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Patent 7,162,549

Figure 11 depicts an embodiment described by Kobayashi. In the embodiment depicted in Figure 11, flash-memory cards 13 both with and without controllers may be used. *Id.* at 12:59-65. Sensor 133 determines the type of flash-memory card 13 mounted on connector 125. *Id.* at 12:59-13: 2. When a flash-memory card with no controller is detected, selector 134 connects ATA controller 124 and connector 125. *Id.* at 13:2-5. When a flash-memory card with a controller is detected, selector 134 connects conversion controller 122 and connector 125.

#### *D. Overview of Kikuchi*

Kikuchi describes a flash-memory card and controller 10 having an interface connected to host computer 14. Ex. 1007, Abstract. Figure 1 of Kikuchi is reproduced below.

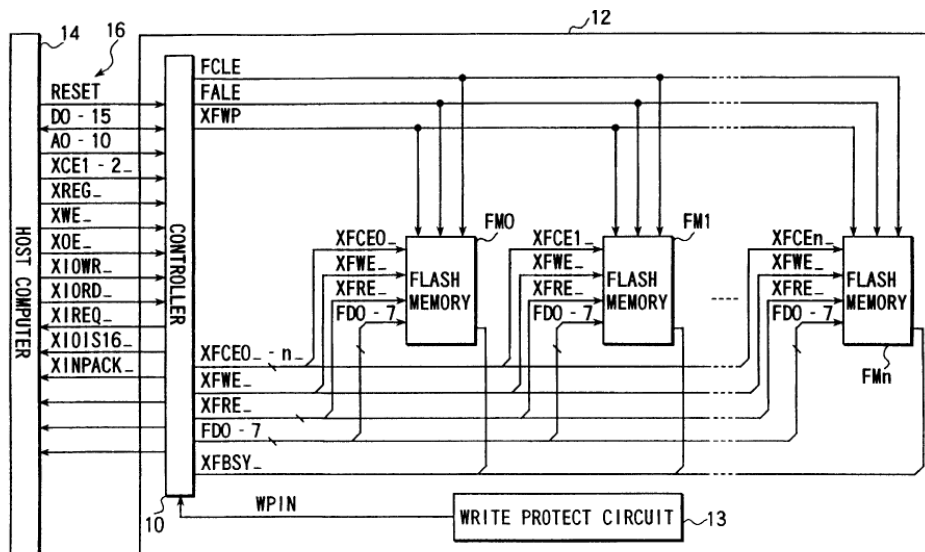


FIG. 1

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Patent 7,162,549

Figure 1 shows the flash memory card with “one-chip controller” 10 on the flash-memory card. *Id.* at 9:10-15<sup>1</sup>. Figure 2 of Kikuchi is reproduced below.

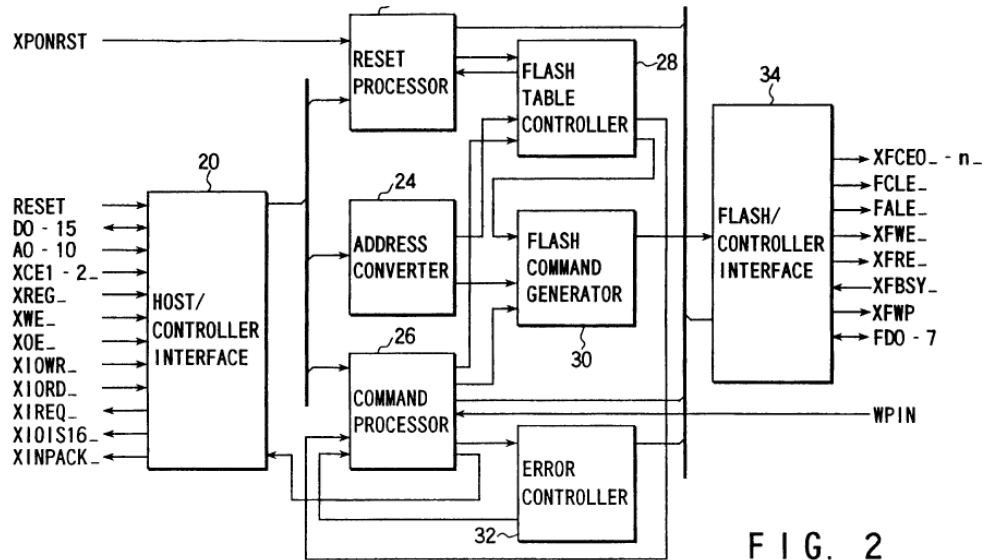


Figure 2 is a block diagram showing the functional arrangement of controller 10, including error controller 32, that performs error control for read and write operations. *Id.* at 11:14-20; 13:17-19. Error controller 32 also “performs a block substituting process or the like in the event of a failure or error.” *Id.* at 13:17-21. In a separate embodiment, controller 10 “refers to the block quality flag contained in the block status information of the redundant portion of the readout information . . . to check whether the head block BL0 is non-defective or not” and “detects a non-defective block BLj having the highest address rank.” *Id.* at 20:20-21:5.

#### *E. Obviousness over Kobayashi and Kikuchi*

HP asserts that a person of ordinary skill in the art would have found the challenged claims obvious over the combination of Kobayashi and

<sup>1</sup> In this opinion, page numbers for this exhibit refer to the number at the right hand bottom of the page, not the number in the top middle of the page.

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Kikuchi. Pet. 42-57 (citing Ex. 1008 (Declaration of Dr. Sanjay Banerjee) ¶¶ 102-122). In particular, HP asserts that Kobayashi discloses every limitation of the challenged claims except the details of error correction. *Id.* at 47-48. HP relies on Kikuchi as describing the recited error correction. *Id.* at 48-49. In addition, HP asserts that it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of the two references, which both describe ATA controllers that work with flash-memory cards with, or without, on-card controllers, in order to “reliably retain stored data.” Pet. 50 (citing Ex. 1008 ¶ 121 (quoting Ex. 1007 (Kikuchi), 4:1-3)).

We are persuaded that a preponderance of the evidence demonstrates that the combination of Kobayashi and Kikuchi discloses each of the limitations of the challenged claims, as presented in HP’s Petition. *See* Pet. 42-57; Ex. 1008 ¶¶ 102-122. We are also persuaded that a preponderance of the evidence demonstrates that a person of ordinary skill in the art would have combined the Kobayashi and Kikuchi references. *See* Pet. 50; Ex. 1008 ¶ 121.

MCM explicitly addresses only the requirement of “a controller chip,” arguing that Kobayashi does not disclose using a single chip with the claimed functionality, but instead has “multiple chips that perform distinct functions.” PO Resp. 14. Specifically, MCM argues that Kobayashi discloses two controllers as separate chips: 122 that exclusively interfaces with cards having controllers, and 124 that exclusively interfaces with cards that do not have controllers. PO Resp. 22. Based on this assertion, MCM argues (1) that the Petition should be dismissed because HP did not point out the single chip requirement explicitly in the Petition (*id.* at 14-21), and

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(2) that the combination of Kobayashi and Kikuchi would not yield the claimed invention, which requires a single chip (*id.* at 21-24). We do not find either argument persuasive.

First, we are persuaded that HP sufficiently discussed the single-chip limitation in its Petition. The Petition explicitly points to Kikuchi's disclosure of "controller 10 as a single chip controller." Pet. 49 (citing Ex. 1007, 7:10-22, 9:11-19); *see also* Pet. 48, 53, 55; Ex. 1008 ¶¶ 114-117. Moreover, Petitioner also asserts that "Kobayashi's controller 122 is a 'one-chip microprocessor.'" Pet. 44 (quoting Ex. 1006, 5:66-6:4, 6:12-22); *see also* Pet. 53, 55. These statements, combined with HP's assertion that combining the teachings of the two references is merely "a combination of prior art elements according to known methods to yield predictable results" (Pet. 50-51), were sufficient for us to determine that Petitioner had a reasonable likelihood of showing unpatentability of the challenged claims. Decision 14-16. We are not persuaded otherwise by Patent Owner's post-institution arguments.

Second, this evidence supports a determination that one of ordinary skill in the art would have had both the knowledge and the inclination to place the functionality taught by Kobayashi and Kikuchi on a single chip. *See* Ex. 1007, 7:12-15 ("This flash memory card has a one-chip controller. . . ."); Ex. 1008 ¶¶ 122-23. In fact, MCM conceded at the oral hearing that it was not beyond the skill of one of ordinary skill at the time of the invention to put multiple functions into a single chip and that, in fact, it is common practice to do so.

JUDGE PERRY: Counsel, are you saying that it is beyond the skill of one of ordinary skill at the time of this invention to put multiple functions integrated into a single chip?

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MR. HELLER: Not at all.

JUDGE PERRY: You are not saying that?

MR. HELLER: Not at all when you have a motivation to do so.

JUDGE PERRY: Isn't it kind of a common practice for those who design integrated circuits to put multiple functions into those circuits?

MR. HELLER: It probably is common practice, but they have to have a motivation to do so.

JUDGE BISK: Is there some reason not to put them on a single chip? It seems like it is just a design choice, whether it is one chip, two chips, 10 chips. Is there a particular reason why the number of chips matters?

MR. HELLER: It is not that. It is, why would you do that? Why would you put all that functionality into a single chip?

Paper 30 ("Tr."), 30:17-31:4.

MCM's assertion—that even if Kikuchi's error correction is incorporated into Kobayashi's ATA controller 124 the result would not yield the claimed invention—misses the point. PO Resp. 20. The relevant inquiry is whether the claimed subject matter would have been obvious to those of ordinary skill in the art in light of the combined teachings of the references. *See In re Keller*, 642 F.2d 413, 425 (CCPA 1981). "Combining the *teachings* of references does not involve an ability to combine their specific structures." *In re Nievelt*, 482 F.2d 965, 968 (CCPA 1973). Patent Owner does not argue that applying the teachings of Kikuchi and Kobayashi so that the claimed functionality is on a single chip would have been "uniquely challenging or difficult for one of ordinary skill in the art" at the time of the invention. *Leapfrog Enters., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157, 1162 (Fed. Cir. 2007) (citing *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007)).

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We conclude that a preponderance of the evidence demonstrates that claims 7, 11, 19, and 21 are unpatentable based on the combination of Kobayashi and Kikuchi.

### III. CONCLUSION

Petitioner has shown, by a preponderance of the evidence, that the challenged claims would have been obvious over the combination of Kobayashi and Kikuchi.

Accordingly, it is

ORDERED that claims 7, 11, 19, and 21 of the '549 patent are determined to be *unpatentable*;

FURTHER ORDERED that because this is a final written decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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Patent 7,162,549

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Paper 19  
Entered: October 10, 2013

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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HEWLETT-PACKARD COMPANY  
Petitioner

v.

TECHNOLOGY PROPERTIES LIMITED LLC,  
and MCM PORTFOLIO LLC  
Exclusive Licensee and Patent Owner

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Patent 7,162,549

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Before JONI Y. CHANG, GLENN J. PERRY, and JENNIFER S. BISK,  
*Administrative Patent Judges.*

BISK, *Administrative Patent Judge.*

DECISION  
Request for Rehearing  
37 C.F.R. § 42.71(d)

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Patent 7,162,549

## SUMMARY

Patent Owner, MCM Portfolio LLC (“MCM”), requests rehearing of the Board’s decision (Paper 10) (“Decision”), entered September 10, 2013, instituting *inter partes* review of claims 7, 11, 19, and 21 of U.S. Patent 7,162,549 (Ex. 1001). Paper 13 (“Rehearing Req.”). For the reasons that follow, MCM’s request for rehearing is *denied*.

## DISCUSSION

The applicable standard for granting a request for rehearing is abuse of discretion. The requirements are set forth in 37 C.F.R. § 42.71(d), which provides in relevant part:

A party dissatisfied with a decision may file a request for rehearing, without prior authorization from the Board. The burden of showing a decision should be modified lies with the party challenging the decision. The request must specifically identify all matters the party believes the Board misapprehended or overlooked, and the place where each matter was previously addressed in a motion, an opposition, or a reply.

MCM argues that a Federal Circuit decision issued subsequent to the filing of the Preliminary Response (Paper 9, filed June 28, 2013) requires the Board to reconsider its decision that 35 U.S.C. § 315(b) does not bar institution of *inter partes* review based on HP’s Petition. Rehearing Req. 3. Specifically, the Board determined that MCM’s assertion that HP and Pandigital are successive owners of the same allegedly infringing property was not enough to support the existence of privity between HP and Pandigital for purposes of § 315(b). Decision 7-8.

In its Request for Rehearing, MCM argues that the Federal Circuit’s August 29, 2013, decision in *Aevoe Corporation v. AE Tech Company, LLC*, mandates that *inter partes* review not be instituted. Rehearing Req. 3-4 (citing *Aevoe Corp. v. AE Tech Co.*, 2013 WL 4563014 (Fed. Cir. 2013)). In particular,

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MCM suggests that *Aevoe* requires the Board to consider, on the issue of privity, MCM's notice to HP that HP's sales of products manufactured by Pandigital were infringing MCM's patent and the subsequent notice to HP of the Texas Action against Pandigital involving those products. Rehearing Req. 3-4.

We do not agree that *Aevoe* requires a reconsideration of our decision regarding lack of privity. *Aevoe* involves an order that enjoined AE Tech and its agents from the "making, manufacturing, importing, offering for sale, selling, and/or otherwise using" a particular patent. *Aevoe*, 2013 WL 4563014 at \*3. Thus, the privity relationship at issue in that case was one related to the infringing products and the reach of the governing injunction. *Id.* at \*8 ("[B]y virtue of their distribution agreement, the S&F Defendants were 'privies' of AE Tech, did not act independently of AE Tech, and were, thus, subject to the original injunction. *See Golden State Bottling Co.* 414 U.S. at 179, 94 S. Ct. 414 (stating that a purchaser acquiring property with knowledge that the wrong enjoined remained unremedied is considered in privity for purposes of Rule 65(d)).").

As we have explained, privity is a contextual concept. *Synopsys v. Mentor Graphics Corp.*, IPR2012-00042, Decision to Institute, Paper 16 at 17 (Feb. 22, 2013). The facts and circumstances present in *Aevoe* are not present here. The allegedly infringing products referred to by MCM are not at issue in this proceeding. Thus, we are not persuaded that *Aevoe* requires that we reconsider our decision that MCM has failed to show that HP and Pandigital are privies for purposes of this proceeding.

MCM makes several other arguments relating to the issue of privity and the § 315(b) bar, but does not identify any arguments or evidence that it asserts the

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Board misapprehended or overlooked.<sup>1</sup> See Rehearing Req. 9-15; 37 C.F.R.

§ 42.71(d). A request for rehearing is not an opportunity to express disagreement with a decision.

MCM's request for rehearing is *denied*.

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<sup>1</sup> We agree with MCM that there is a typographical error on page 8 of the Decision. The sentence “*Petitioner* provides no persuasive evidence that HP could have exercised control over Pandigital’s participation in the Texas Action” should read “*Patent Owner* provides no persuasive evidence that HP could have exercised control over Pandigital’s participation in the Texas Action.” Decision 8 (emphases added). However, this does not change the outcome of either the Decision or this decision on request for rehearing. An errata correcting the typographical error will be issued simultaneously with this decision.

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Paper 10  
Entered: September 10, 2013

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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HEWLETT-PACKARD COMPANY  
Petitioner

v.

MCM PORTFOLIO, LLC  
Patent Owner

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Case IPR2013-00217  
Patent 7,162,549

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Before SCOTT R. BOALICK, JONI Y. CHANG, and JENNIFER S. BISK,  
*Administrative Patent Judges.*

BISK, *Administrative Patent Judge.*

DECISION  
Institution of *Inter Partes* Review  
*37 C.F.R. § 42.108*

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Patent 7,162,549

## I. INTRODUCTION

*A. Background*

Hewlett-Packard Company (“HP”) filed a petition (Paper 2) (“Pet.”) to institute an *inter partes* review of claims 7, 11, 19, and 21 of Patent 7,162,549 (the “’549 patent”). 35 U.S.C. § 311. MCM Portfolio, LLC (“MCM”) timely filed a Preliminary Response (Paper 9) (“Prelim. Resp.”). We conclude that HP has satisfied its burden to show that, under 35 U.S.C. § 314(a), there is a reasonable likelihood that it would prevail with respect to at least one of the challenged claims.

HP contends that the challenged claims are unpatentable under 35 U.S.C. §§102 and/or 103 based on the following specific grounds (Pet. 7):

Reference[s] <sup>1</sup>	Basis	Claims challenged
AwYong	§ 102	7, 11, 19, and 21
Battaglia	§ 103	7, 11, 19, and 21
Battaglia and the Samaung Datasheet	§ 103	7, 11, 19, and 21
Kobayashi and Kikuchi	§ 103	7, 11, 19, and 21

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<sup>1</sup> U.S. Patent 6,987,927 (Ex. 1004) (“Battaglia”); U.S. Patent 6,199,122 (Ex. 1005) (“Kobayashi”); WO 98/03915 (Ex. 1007) (“Kikuchi”); Chee-Kong AwYong, An Integrated Control System Design of Portable Computer Storage Peripherals, Master’s Thesis, National Chiao-Tung University, published Dec. 22, 2000 (Ex. 1003) English Translation (Ex. 1002) (“AwYong”); Samsung SmartMedia Card Model No. K9D1208V0M-SSB0 Datasheet (Nov. 20, 2000) (Ex. 1006) (“Samsung Datasheet”).

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For the reasons described below, we institute an *inter partes* review of claims 7, 11, 19, and 21 based on obviousness over Kobayashi combined with Kikuchi.

We decline to institute *inter partes* review based on the following grounds: (1) anticipation by AwYong; (2) obviousness over Battaglia; and (3) obviousness over Battaglia combined with the Samsung Datasheet.

*B. Related Proceedings*

The parties list several cases pending in the Eastern District of Texas that would affect or be affected by the decision in this proceeding, including *Technology Properties Limited, LLC v. Hewlett-Packard Co.*, Docket No. 6:12-cv-208 (E.D. Tex. Mar. 28, 2012), in which the '549 patent is asserted against Petitioner. *See* Pet. 1; Paper 6 at 1. That case currently is stayed pending resolution of a related proceeding before the United States International Trade Commission ("ITC") that also involves the '549 patent, ITC Inv. No. 337-TA-841. *Id.* In addition, the '549 patent is the subject of a pending reissue proceeding, U.S. Application No. 12/351,691. The Board ordered a stay of that proceeding pending the termination or completion of this proceeding. Paper 8.

*C. The Invention*

The '549 patent relates to controllers for flash-memory cards. Ex. 1001, col. 1, ll. 21-22. As described in the "Background of the Invention," at the time of the invention, removable flash-memory cards commonly were used with digital cameras to allow for convenient transfer of images from the camera to a personal computer. *Id.* at col. 1, ll. 26-56. These prior art flash-memory cards were available in several formats, including CompactFlash, SmartMedia, MultiMediaCard (MMC), Secure Digital Card (SD), and Memory Stick card. *Id.* at col. 2, ll. 28-55. Each of the card formats required a different interface adapter

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to work with a personal computer. *Id.* at col. 3, ll. 9-25. The Specification describes a need for a flash-memory card reader that accepts flash-memory cards of several different formats using a universal adapter. *Id.* at ll. 52-63. In response to this need, the '549 patent describes various improvements to flash-memory card readers, including by determining whether a particular flash-memory card includes a controller, and if not, performing operations to manage error correction for the flash-memory card. *Id.* at col. 3, l. 53- col. 4, l. 26; col. 28, ll. 42-60.

Claims 7 and 11, reproduced below, are illustrative of the claimed subject matter:

7. A method comprising:

using a controller chip to interface a flash storage system with or without a controller to a computing device, the controller chip comprising a flash adapter, wherein the flash storage system comprises a flash section and at least a medium ID;

determining whether the flash storage system includes a controller for error correction; and

in an event where the flash storage system does not have a controller for error correction, using firmware in the flash adapter to perform operations to manage error correction of the flash section, including bad block mapping of the flash section in the flash storage system that is coupled to the flash adapter section.

11. A system comprising:

a computing device;

a flash storage system comprising a flash section and at least a portion of a medium ID; and

a controller chip coupled between the computing device and the flash storage system to interface the flash storage system to the computing device, the controller chip comprising an interface mechanism capable of receiving flash storage systems with controller and controllerless flash storage systems, a detector to determine whether the flash storage system includes a controller

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for error correction and a flash adapter which comprises firmware to perform, in an event where the flash storage system does not have a controller for error correction, operations to manage error correction of the flash section, including bad block mapping of the flash section in the flash storage system that is coupled to the flash adapter section.

#### *D. Claim Construction*

As a step in our analysis for determining whether to institute a trial, we determine the meaning of the claims. Consistent with the statute and the legislative history of the AIA, the Board will interpret claims using the broadest reasonable construction. *See* 37 C.F.R. § 42.100(b); *Office Patent Trial Practice Guide*, 77 Fed. Reg. 48756, 48766 (Aug. 14, 2012).

##### *1. “Flash Adapter” and “Flash Adapter Section”*

HP proposes that the broadest reasonable construction of “flash adapter” and “flash adapter section” is that adopted in the related ITC Investigation—“a section of the controller chip that enables communication with the flash storage system.” Pet. 8 (citing Ex. 1030, pp. 73-77). MCM agrees with that construction. Prelim. Resp. 11. We find that this definition is reasonable and supported by the claim language, and thus adopt this definition for purposes of this decision.

##### *2. “Error Correction” and “Bad Block Mapping”*

HP does not set forth an explicit construction for the terms “error correction” or “bad block mapping.” MCM, however, argues that HP incorrectly construes the term “bad block mapping” as distinct from “error correction.” Prelim. Resp. 11. (citing Ex. 1008 (“Banjeree Decl.”) ¶ 28). MCM instead proposes a construction of the term used by the examiner during original prosecution—“bad block mapping is a form of error correction.” Prelim. Resp. 11-12 (citing Ex. 1015 at 415).

“Bad block mapping” is not defined explicitly in the written description of

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the '549 patent. The plain and ordinary meaning of “bad block” is “a faulty memory location.” MICROSOFT COMPUTER DICTIONARY 41 (4th ed. 1999). The plain and ordinary meaning of “a memory map” is “a description of the layout of objects in an area of memory.” *Id.* at 281. Thus, the plain and ordinary meaning of “bad block mapping” is a description of the layout of those faulty memory locations, kept so that they are not accessed. Under a broadest reasonable construction, bad block mapping is thus a type of error correction.

This construction also is consistent with the Specification, which states that “the primary reason for including a controller section in a flash medium is for error correction. This task is now shifted either to firmware 4012*b* of the host computer, which now on top of its normal access section software, also manages error correction and bad block mapping of chip(s) 4022 and stores those parameters in flash medium 4020*b* itself.” Ex. 1001, col. 28, ll. 53-58. This is the only place, outside the claims, that the term “bad block mapping” is used in the '549 patent. However, the claim language also supports this construction. Claim 7 recites “using firmware in the flash adapter to perform operations to manage error correction of the flash section, including bad block mapping of the flash section,” and claim 11 recites “operations to manage error correction of the flash section, including bad block mapping of the flash section.”

For these reasons, for purposes of this decision, we construe the term “bad block mapping” to be a type of “error correction.”

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## II. ANALYSIS

### A. 35 U.S.C. § 315(b)

MCM argues that institution of an *inter partes* review is barred under 35 U.S.C. § 315(b).<sup>2</sup> Section 315(b) states as follows:

An inter partes review may not be instituted if the petition requesting the proceeding is filed more than 1 year after the date on which the petitioner, real party in interest, or privy of the petitioner is served with a complaint alleging infringement of the patent.

MCM asserts that Pandigital, Inc. is a privy of HP and, therefore, a complaint served on Pandigital by MCM in 2011, more than one year prior to the filing of the Petition in this case, filed by HP on March 27, 2012, should trigger § 315(b).

Prelim. Resp. 5 (citing Ex. 2001 (*Technology Properties Limited LLC v. Pandigital, Inc.*, No. 2:11-cv-00372-TJW (E.D. Tex. 2011) (the “Texas Action”))). MCM bases this allegation on the fact that HP resells Pandigital products accused of infringing the ’549 patent in the Texas Action. *Id.* at 5-6 (citing Ex. 2003 at 20 (HP User Guide)). According to MCM, the Petition in this case is filed more than one year after service of the complaint on Pandigital, a privy of HP. Prelim. Resp. 5-9.

MCM does not provide persuasive evidence that HP and Pandigital are privies for purposes of § 315(b). “Whether a party who is not a named participant in a given proceeding nonetheless constitutes a ‘real party-in-interest’ or ‘privy’ to that proceeding is a highly fact-dependent question.” *Office Patent Trial Practice Guide*, 77 Fed. Reg. 48759 (citing *Taylor*, 553 U.S. 880). “The Office intends to

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<sup>2</sup> MCM asserts that HP “lacks standing” to bring this IPR. Standing technically is not a requirement in an IPR. See, e.g., *Office Patent Trial Practice Guide*, Fed. Reg. at 48759 (“[The notion of ‘real party-in-interest’] reflects standing concepts, but no such requirement exists in the IPR or PGR context.”).

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evaluate what parties constitute ‘privies’ in a manner consistent with the flexible and equitable considerations established under federal caselaw.” *Id.* Petitioner provides no persuasive evidence that HP could have exercised control over Pandigital’s participation in the Texas Action. Thus, § 315(b) does not bar institution of *inter partes* review based on HP’s Petition.

MCM bases its privity argument solely on its assertion that HP and Pandigital are successive owners of the same allegedly infringing property. Prelim. Resp. 7 (citing *Taylor v. Sturgell*, 553 U.S. 880, 894 (2008)). We are not persuaded that this allegation alone is enough to confer privity for purposes of § 315(b). See *Synopsys v. Mentor Graphics Corp.*, IPR2012-00042, Decision to Institute, Paper 16 (Feb. 22, 2013) (“*Synopsis*”). Under *Synopsis* “any potentially infringing products are irrelevant to the issues raised in the Petition, all of which involve patentability.” *Synopsis* at 17.

*B. Priority Date for the ’549 Patent Claims*

The ’549 patent claims the benefit of one provisional application and is a continuation-in-part of four non-provisional applications. Ex. 1001, col. 1, ll. 6-17; Certificate of Correction (Jan. 9, 2007). MCM asserts that the effective filing date of the challenged claims is the earliest filing date of these applications—application No. 09/610,904, filed July 6, 2000 (now U.S. Patent 6,438,638) (the “’904 application”). Prelim. Resp. 17-18. HP, on the other hand, asserts that the challenged claims are entitled to an effective filing date no earlier than June 4, 2002. Pet. 3.

In this case, the effective filing date of the ’549 patent (i.e., whether it is entitled to the benefit of the ’904 application’s filing date) is relevant because several of the asserted references post-date the filing date of the ’904 application. In particular, although AwYong is stamped with a date of June 2000, HP states that

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it was “published and publicly available as of December 22, 2000,” several months after the filing of the ’904 application. In addition, Battaglia has a filing date of July 13, 2000, and HP states that the Samsung Datasheet was available by November 20, 2000—both of which are after the ’904 application’s filing date.

HP provides little explanation regarding its proposed effective date, basing its entire argument on the statement that “[i]n the related ITC Investigation, the Patent Owner’s exclusive licensee – Technology Properties Limited, LLC (‘TPL’) – agreed that June 4, 2002 is the effective filing date of the ’549 Patent.” Pet. 3 (citing Ex. 1008 (“Banerjee Decl.”) ¶ 33). HP does not explain why the actions of MCM’s licensee in another proceeding would be applicable here; nor does HP provide any evidence, aside from one conclusory statement by an expert, Dr. Banerjee, to support this assertion. *Id.*

Other than the conclusory statement regarding the related ITC Investigation, we find no other evidence in the record<sup>3</sup> to support the proposed 2002 effective date except the testimony of Dr. Banerjee, who states that “Claims 7, 11, 19, and 21 of the ’549 Patent are entitled to a priority date of no earlier than June 4, 2002” because the concepts of interfacing with “intelligent” and “dumb” flash cards do not appear until a provisional application on June 4, 2002. Ex. 1008 ¶¶ 33-34. HP, however, does not provide any of the underlying evidence upon which these conclusions are based. We, therefore, give them minimal weight. 37 C.F.R. § 42.65. None of the applications to which the ’549 patent claims benefit have been entered into the record in this case. Moreover, Dr. Banerjee’s statement does not refer to all those applications. Specifically, Dr. Banerjee does not mention the

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<sup>3</sup> HP did not cite to any other testimony in its Petition, but MCM does refer to other testimony by disputing that testimony in its response. Prelim. Resp. 17-18.

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'904 application, included in the certificate of correction, which has the earliest filing date—July 6, 2000; instead, he specifically discusses only the applications listed in the first column of the '549 patent. *Id.* at ¶ 34. Thus, it is unclear from the testimony whether Dr. Banerjee studied or was aware of the earliest claimed application.

Because we are not persuaded by HP's contention that the challenged claims are not entitled under 35 U.S.C. § 120 to the benefit of the filing date of the '904 application, HP has not shown sufficiently that AwYong, Battaglia, or the Samsung Datasheet are eligible as prior art for purposes of this decision. Thus, we decline to institute *inter partes* review based on any of those references.

*C. Obviousness over Kobayashi and Kikuchi*

HP argues that claims 7, 11, 19, and 21 of the '549 patent are obvious over Kobayashi combined with Kikuchi. Both Kobayashi and Kikuchi pre-date the filing date of the '904 application. Kobayashi is a U.S. patent that was filed July 22, 1998 and Kikuchi is a PCT application published January 29, 1998.

*1. Kobayashi*

Kobayashi describes a memory device for a computer with a converter that converts serial commands of the computer to parallel commands that then are used to control a storage medium (which can be a flash-memory card). Ex. 1005, col. 2, ll. 55-64; col. 3, ll. 63-65. This configuration is shown in Figure 1.

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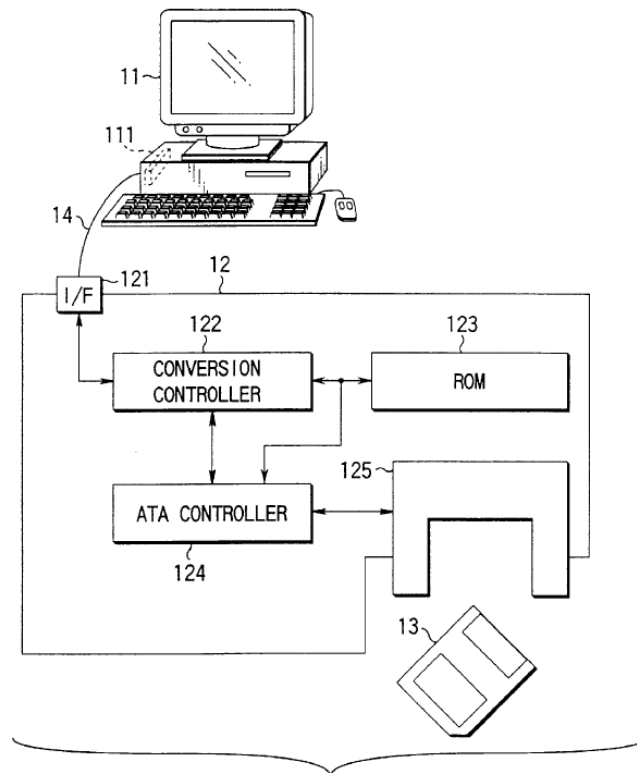


FIG. 1

Figure 1 of Kobayashi, reproduced above, is a block diagram of a computer 11 with a reader/writer 12 and flash-memory card 13. Ex. 1005, col. 5, ll. 54-58. The reader/writer includes a conversion controller 122, an ATA (AT Attachment) controller 124, and a connector 125 for reading a flash-memory card 13. *Id.* at col. 6, ll. 5-9. In the first of several embodiments described by Kobayashi, the flash-memory card 13 does not have a controller on the card. *Id.* at col. 6, ll. 1-4 (“The memory card 13 functions as what is called a silicon disk or a PC card according to the ATA standard, and stores data and reads, outputs and erases the stored data under an *external control*.”) (emphasis added). A second embodiment described by Kobayashi includes a flash-memory card 13 with a controller arranged in the memory card. *Id.* at col. 12, ll. 44-46, 59-63. A third embodiment is shown in Figure 11.

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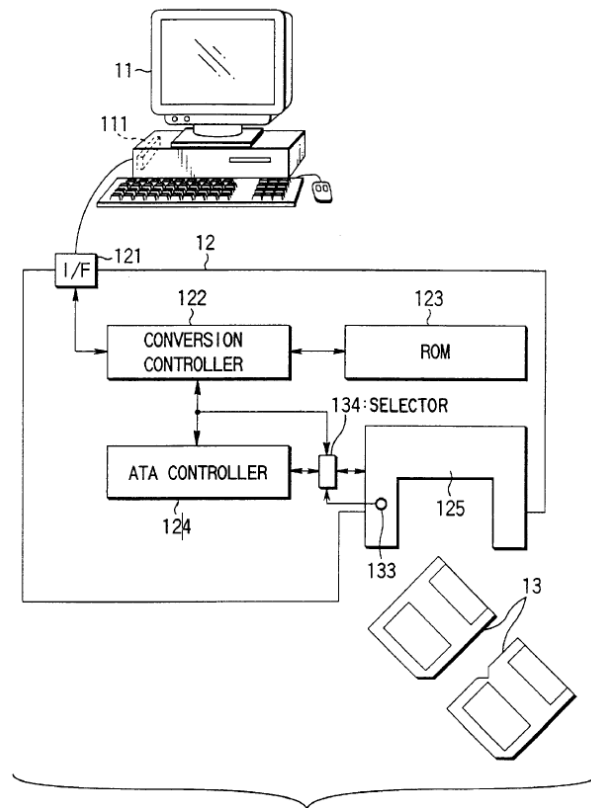


FIG. 11

In this third embodiment, flash-memory cards 13 both with and without controllers may be used. *Id.* at col. 12, ll. 59-65. A sensor 133 determines the type of flash-memory card 13 mounted on the connector 125. *Id.* at col. 12, l. 59 – col. 13, l. 2. When a flash-memory card with no controller is detected, a selector 134 connects the ATA controller 124 and the connector 125. *Id.* at col. 13, ll. 2-5. When a flash-memory card with a controller is detected, a selector 134 connects the conversion controller 122 and the connector 125.

## 2. Kikuchi

Kikuchi describes a flash-memory card and a controller 10 having an interface connected to a host computer 14. Ex. 1007, Abstract. Figure 1 of Kikuchi, reproduced below, shows the flash memory card with a controller on the

FIG. 1 is a block diagram of a multi-ported flash memory system. A host computer (14) is connected to a controller (10) via a bus (12). The controller (10) manages multiple flash memory units (FM0, FM1, ..., FMn). Each unit has its own set of control signals (XFCE, XFWE, XFRE, FDO) and a write protect pin (WPIN) connected to a write protect circuit (13).

Figure 15A of Kikuchi, reproduced below, shows a flash-memory card with no controller. Ex. 1007, p. 33, ll. 22-25.

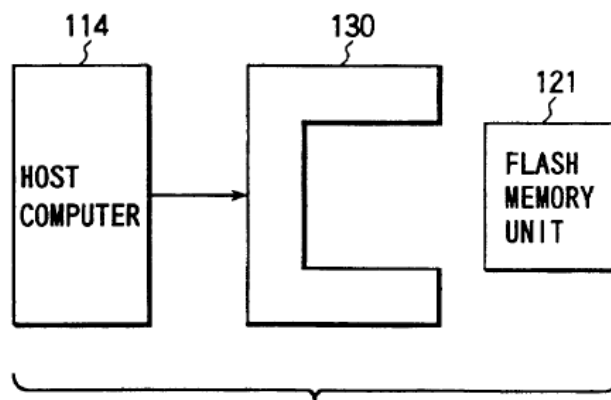


Figure 2, reproduced below, is a block diagram showing the functional

Case IPR2013-00217

Patent 7,162,549

arrangement of the controller 10.

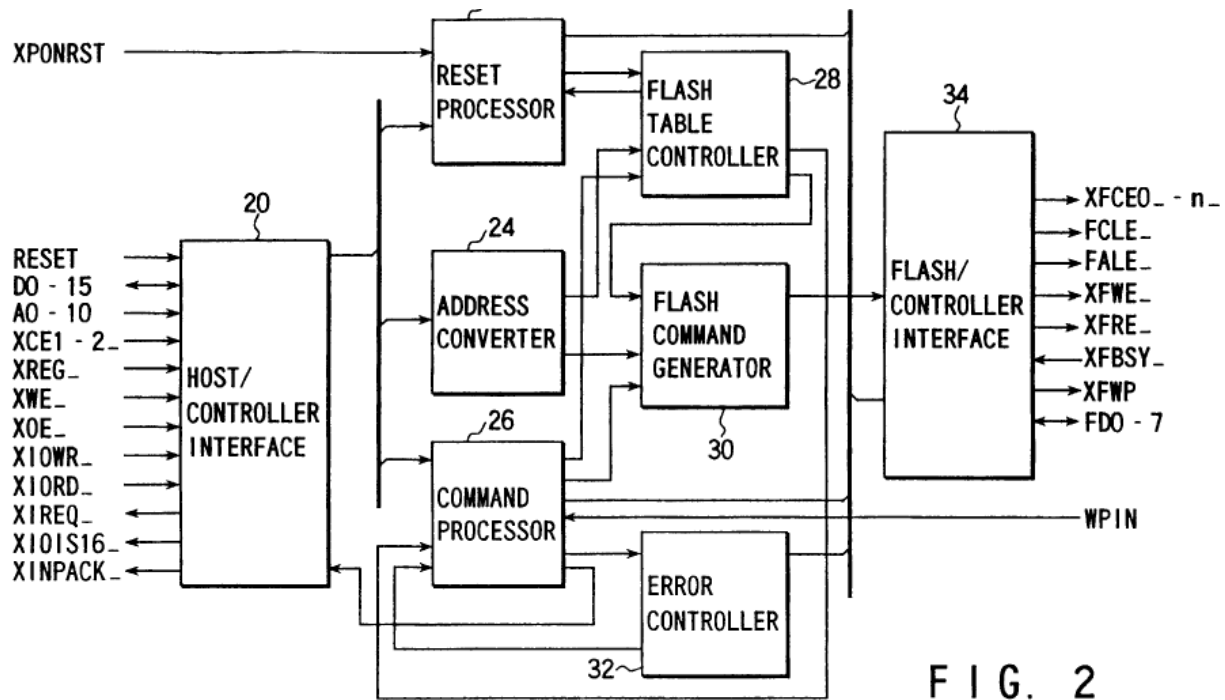


FIG. 2

In Figure 2, above, the error controller 32 performs error control in read and write operations and performs bad block mapping, for example, “a block substitute process or the like in the event of a failure or error.” Ex. 1007, p. 13, ll. 17-21. Further, in another embodiment, controller 10 “refers to the block quality flag contained in the block status information of the redundant portion of the readout information . . . to check whether the head block BL0 is non-defective or not” and “detects a non-defective block BLj having the highest address rank.” *Id.* at p. 22, l. 20 – p. 23, l. 5.

### 3. The Combination of Kobayashi and Kikuchi

HP asserts that Kobayashi discloses every limitation recited by all the challenged claims, except that HP concedes that Kobayashi is silent on the details of how error correction is performed and, in particular, does not mention bad block mapping. Pet. 47-48. HP relies on Kikuchi for teaching the details of error

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Patent 7,162,549

correction, including bad block mapping, done in firmware. Pet. 48-50. HP contends that it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of the two references, which both describe ATA controllers that work with flash-memory cards with or without on-card controllers, in order to “reliably retain stored data.” Pet. 50 (citing Banerjee Decl. ¶ 121 (quoting Ex. 1007 (Kikuchi), p. 6, ll. 1-3)). We have reviewed HP’s evidence in relation to each of the challenged claims and find that the evidence supports HP’s contentions.

MCM argues that Kobayashi does not disclose using firmware to perform the error correction in the event that the flash-memory card is without a controller, as required by all the challenged claims. Prelim. Resp. 29. This argument is not persuasive because MCM concedes that Kikuchi discloses a controller using firmware to perform error correction. *Id.* at 29-31 (stating that Kikuchi discloses “a controller in a card reader that has a microprocessor that conducts bad block mapping in firmware”).

MCM argues that Kikuchi’s controller chip could not be incorporated into Kobayashi’s controller. Prelim. Resp. 31-32. Moreover, MCM adds that even if Kikuchi’s controller chip could be incorporated into Kobayashi’s controller, it would not yield the claimed invention because Kobayashi discloses two controllers—a conversion controller 122 and an ATA controller 124—not one controller chip with all the required functionality. Prelim. Resp. 33-34.

Neither argument is persuasive. “It is well-established that a determination of obviousness based on teachings from multiple references does not require an actual, physical substitution of elements.” *In re Mouttet*, 686 F.3d 1322, 1332 (Fed. Cir. 2012) (citing *In re Etter*, 756 F.2d 852, 859 (Fed. Cir. 1985) (en banc) (noting that the criterion for obviousness is not whether the references can be

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combined physically, but whether the claimed invention is rendered obvious by the teachings of the prior art as a whole)). On this record, we determine that the petition and supporting evidence demonstrate sufficiently that combining the teachings of Kobayashi and Kikuchi merely is a predictable use of prior art elements according to their established functions—an obvious improvement. *See KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007).

Finally, MCM argues that Kobayashi was considered by the Examiner during prosecution (Prelim. Resp. 25) and Kikuchi is cumulative of art that was before the Examiner during prosecution (Prelim. Resp. 29-30). While we are mindful of the burden on MCM and the Office in analyzing previously considered prior art, substantially the same prior art and arguments were not before the Office previously. *See* 35 U.S.C. § 325(d). Moreover, for the reasons explained above, we conclude that HP’s arguments based on the combination of Kobayashi and Kikuchi have merit.

### III. CONCLUSION

We institute an *inter partes* review of claims 7, 11, 19, and 21 based on obviousness over Kobayashi combined with Kikuchi.

### IV. ORDER

For the reasons given, it is

**ORDERED** that the Petition is granted as to claims 7, 11, 19, and 21 of the ’549 patent on the alleged ground of obviousness over Kobayashi combined with Kikuchi under 35 U.S.C. § 103.

**FURTHER ORDERED** that pursuant to 35 U.S.C. § 314(a), *inter partes* review of the ’549 patent hereby is instituted commencing on the entry date of this Order, and pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice

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Patent 7,162,549

hereby is given of the institution of a trial.

**FURTHER ORDERED** that an initial conference call with the Board is scheduled for **2 PM Eastern Time on October 9, 2013**. The parties are directed to the *Office Trial Practice Guide*, 77 Fed. Reg. at 48765-66 for guidance in preparing for the initial conference call, and should come prepared to discuss any proposed changes to the Scheduling Order entered herewith and any motions the parties anticipate filing during the trial.

PETITIONER:

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/351,691	01/09/2009	Sreenath Mambakkam	76706-201401-R1	9332
73481	7590	11/05/2014	EXAMINER	
Alliacense Limited LLC			CHEN, ALAN S	
4880 Stevens Creek Boulevard				
Suite 103				
San Jose, CA 95129				
			ART UNIT	PAPER NUMBER
			2129	
			NOTIFICATION DATE	DELIVERY MODE
			11/05/2014	ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

emi@alliacense.com  
joanna@alliacense.com  
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ALLIACENSE Limited LLC  
4880 STEVENS CREEK BOULEVARD  
SUITE 103  
SAN JOSE, CA 95129

*In re* Application of:  
Mambakkam, et al.  
Appl. No.: 12/351,691  
Attorney Docket No. 76706-201401-R1  
Filed: January 09, 2009  
For: MULTIMODE CONTROLLER FOR INTELLIGENT AND  
“DUMB” FLASH CARDS

**REOPENING OF  
PROSECUTION IN  
ACCORDANCE WITH PTAB  
ORDER LIFTING STAY**

In accordance with the ORDER from the PTAB entered September 12, 2014 in U.S. Patent No. 7,162,549, which is relevant to the examination of this application, the stay of the concurrent examination of the instant reissue application ('691) is lifted. Note, on August 6, 2014, a Final Written Decision under 35 U.S.C. § 318(a), determining claims 7, 11, 19 and 21 of the '549 patent to be unpatentable (see paper 31 therein).

Accordingly, a response period of (2) two-months is set, beginning on the mailing date of this decision, in which to file an Appeal Brief in accordance with 37 CFR § 41.37. Applicant is reminded if the appeal results in an examiner's answer, the appeal forwarding fee set forth in § 41.20(b)(4) must be paid within the time period specified in § 41.45 to avoid dismissal of an appeal.

Applicant is also reminded of their duty to disclose any information related to the subject matter of the instant application, as well as the need to file any pertinent amendment(s) in accordance with the Final Written Decision in the inter partes review of Patent No. 7,162,549.

Serial No.: 12/351,691  
Order Lifting Stay

- 2 -

Any inquiry concerning this decision should be directed to the undersigned whose telephone number is (571) 272-3595.

\_\_\_\_\_/Brian Johnson/\_\_\_\_\_  
Brian Johnson, QAS  
Technology Center 2100  
Computer Architecture and Software

**Electronic Acknowledgement Receipt**

<b>EFS ID:</b>	20706080
<b>Application Number:</b>	12351691
<b>International Application Number:</b>	
<b>Confirmation Number:</b>	9332
<b>Title of Invention:</b>	MULTIMODE CONTROLLER FOR INTELLIGENT AND "DUMB" FLASH CARDS
<b>First Named Inventor/Applicant Name:</b>	Sreenath Mambakkam
<b>Customer Number:</b>	73481
<b>Filer:</b>	Edward Peter Heller/Emi Rhodes
<b>Filer Authorized By:</b>	Edward Peter Heller
<b>Attorney Docket Number:</b>	76706-201401-R1
<b>Receipt Date:</b>	14-NOV-2014
<b>Filing Date:</b>	09-JAN-2009
<b>Time Stamp:</b>	17:42:42
<b>Application Type:</b>	Utility under 35 USC 111(a)

**Payment information:**

Submitted with Payment	no
------------------------	----

**File Listing:**

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		76706-201401-R1_Rule4133_141114.pdf	143569 345cd77af47c1822ae40ab621fa5351376db673a	yes	21

	Document Description	Start	End
	Amendment/Argument after Notice of Appeal	1	1
	Specification	2	9
	Claims	10	18
	Applicant Arguments/Remarks Made in an Amendment	19	21

**Warnings:****Information:****Total Files Size (in bytes):**

143569

**This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.**

**New Applications Under 35 U.S.C. 111**

**If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.**

**National Stage of an International Application under 35 U.S.C. 371**

**If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.**

**New International Application Filed with the USPTO as a Receiving Office**

**If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant(s): Mambakkam, Sreenath et al.	Art Unit: 2129
Application No.: 12/351,691	Examiner: Chen, Alan S.
Filed: 1/09/2009	Confirmation No. 9332
Reissue of U.S. 7,162,549	
Title: Multimode Controller for Intelligent and "Dumb" Flash Cards	
Atty Docket No.: 76706-201401-R1	

Mail Stop: Amendment  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

§ 41.33 AMENDMENT

Dear Sir:

Responsive to the notice of the reopening prosecution dated November 5, 2014, please find the following:

- an amendment to the specification begins at page 2;
- a listing of the claims begins at page 10;
- a listing of the status of the claims begins at 18; and
- remarks begin at page 19.

IN THE SPECIFICATION

Please withdraw the amendments to the specification entered in the preliminary amendment of January 9, 2009, and enter the following in lieu thereof.

Please replace paragraph 4 of column 28 (beginning line 27) of the specification with the following amended paragraph:

--Host computer 4000 also typically has driver software 4002, and [adapter chip] controller IC 4010 contains firmware 4012. Flash medium 4020 typically may consist of a controller section 4021 and a flash section 4022. In most cases, these sections are at least two separate ICs, although in some cases they may be integrated into one IC. However, in all cases, there is a significant added cost for the controller section, whether it comprises a separate chip or is integrated into a single IC with the flash section 4022--

Please replace paragraph 5 of column 28 (beginning line 37) of the specification with the following amended paragraph:

--Typically, the purpose of controller 4021 is to present a flawless medium to the system, in a specific format, so the computer 4000 sees an error-free [storage] flash medium 4020, rather than a flash section 4022 that may have certain defects that must be mapped away.--

Please replace paragraph 6 of column 28 (beginning line 42) of the specification with the following amended paragraph:

--FIG. 31 shows an improved flash medium 4020b. Flash medium 4020b still has a flash section or IC 4022, but the controller section 4021 has been removed. Shown now in detail is a medium ID 4030, some aspects of which have been discussed in earlier sections above, and which in some cases may be split between the flash medium and the media adapter cards, as also described earlier. That medium ID 4030 includes in some cases certain basic specifications of the medium, such as the memory type, the total capacity, etc. Originally, the controller 4021 (FIG. 30) was used to provide that kind of information; however, as discussed just above, the primary reason for including a controller section in a flash medium is for error correction. This task is now shifted either to firmware 4012b of the [host computer] controller IC

4010b (having an interface connection 4001 that connects to host computer 4000), which now, on top of its normal access section software, also manages error correction and bad block mapping of [chip(s)] flash section 4022 and stores those parameters in flash medium 4020b itself. Or in some cases, this function may be shifted to driver software 4002b in the host computer 4000.--

Please replace paragraph 6 of column 28 (beginning line 61) of the specification with the following amended paragraph:

--Often this error mapping and other functions may be handled in combination between those two software elements (firmware 4012b and driver software 4002b), or in some cases it may be shifted entirely to firmware 4012b, which allows the driver software [4002] 4002b to remain a standard removable medium driver rather than including specialized firmware. Shifting control entirely to firmware 4012b allows for transparent use of the flash, much as the original controller 4021 (FIG. 30) did. Thus an operating system would not be able to distinguish one from the other, and no special drivers, patches, etc., would have to be installed by the user.--

Please replace paragraph 2 of column 29 (beginning line 5) of the specification with the following amended paragraph:

--[Identification] Medium ID 4030 makes use of those pins discussed in the [sections'] sections above (see FIG. 5, for example), and in all those cases discussed above, a mechanical-electrical medium adapter may be used on [bus] interface 4011 for different electromechanical connection interfaces, etc.--

Please replace paragraph 3 of column 29 (beginning line 10) of the specification with the following amended paragraph:

--FIG. 32 shows various implementations of medium ID 4030. For example, ID 4030a uses simple pull-ups and pull-downs, as discussed earlier. ID 4030b uses, rather than simple pull-ups and pull-downs, voltage dividers, in this example consisting of R2/R3 and R4/R5. By using voltage dividers, a limited number of pins, such as, for example, two, can be stretched into offering 16 or even more different types of cards or IDs, based on the fact that, rather than one bit per pin (high or low), multiple voltage levels (and hence multiple bits) per pin can now

be supported, using voltage dividers, and therefore many more card combinations can be identified through a limited number of pins. On the controller side, Fig. 31, comparators 4028 may be used to regenerate digital signals [(not shown for clarity).] which may be used by firmware 4012b to determine the type of media card present (FIG.s 4A-E and 12A-E), including whether it has a controller 4021. (A CompactFlash brand flash memory card, for example, has a controller. A SmartMedia brand flash memory card does not.)--

Please replace paragraph 4 of column 29 (beginning line 24) of the specification with the following amended paragraph:

--ID 4030c achieves the same result by having a small E<sup>2</sup> programmable ROM as a digital ID. This could be a mask program or E<sup>2</sup>-type serial memory, which is available very inexpensively. The E<sup>2</sup> could be programmed at the factory or in the field through firmware 4012b. Many types of low pin count serial buses are known to the inventor and to those skilled in the art (such as Single Wire<sup>TM</sup> brand bus by Dallas Semiconductor, I<sup>2</sup>C etc.), counting from 1-4 pins including power in some cases. The advantage of using the E<sup>2</sup> would be, for

example, to allow use of a flash [chip] section 4022 that even has a bad boot sector, because a new boot sector address could be incorporated into 4030c, rather than having to rely on the [main storage] flash section 4022 to be error free.--

Please replace paragraph 5 of column 29 (beginning line 37) of the specification with the following amended paragraph:

--As the industry moves to higher and higher single-chip capacity, the chances of having bad sectors in the boot section increase. By moving the boot sector address into an auxiliary device, such as ID 4030c, the yield of usable [chips] memory in flash section 4022 can be dramatically increased, and therefore costs can be further reduced.--

Please replace paragraph 6 of column 29 (beginning line 43) of the specification with the following amended paragraph:

--Also, elimination of the controller 4021 helps to further reduce the cost of medium [4022] 4020b. By having a combined firmware 4012b that can handle both media cards such as flash medium [4022] 4020 with controllers of all formats discussed above and of others not discussed, as well as controller-less media cards such as flash medium

4020b, with [an] medium ID 4030, backward compatibility is guaranteed in the market.--

Please replace paragraph 7 of column 29 (beginning line 50) of the specification with the following amended paragraph:

--Although the present invention has been described in accordance with the embodiments shown, one of ordinary skill in the art will readily recognize that there could be variations to the embodiments and those variations would be within the spirit and scope of the present invention. Accordingly, many modifications may be made by one of ordinary skill in the art without departing from the spirit and scope of the appended claims. Among these modifications and variations, controller IC 4010 may alternatively be located in a host computer, such as PC 20 (Fig. 14), and be connected to a CPU, or be located in a separate flash card reader 42 (Figs. 6 and 13) and connected to a host computer, such as PC 20, by a bus, USB, Ethernet, or IDE connection. Additionally, the information provided by the medium ID 4030 may also be provided by, for example, the flash medium controller 4021. Further, while the description of flash media cards comprises known flash media

types, the description is intended to be generic as to flash media types  
and formats. --

Claims:

1-6. Cancel

7. (Amended) A method comprising:

using a controller chip to interface a flash storage system with or without a controller to a computing device, the controller chip comprising a flash adapter section, wherein the flash storage system comprises a flash section and at least a medium ID;

determining whether the flash storage system includes a controller for error correction; and

in an event where the flash storage system does not have a controller for error correction, using firmware in the flash adapter section to perform operations to manage error correction of the flash section, including bad block mapping of the flash section in the flash storage system that is coupled to the flash adapter section.

8. (Original) The method of claim 7, further comprising: storing specifications of the flash storage system in the medium ID.
9. (Original) The method of claim 7, further comprising updating the specifications in the medium ID during bad block mapping of the flash section, wherein the medium ID comprises one or more EEPROM devices to store the specifications.
10. (Original) The method of claim 7, further comprising examining the medium ID to identify a type of the flash storage system, wherein the medium ID comprises at least one of a pull-up resistor, a pull-down resistor, and a voltage divider.
11. (Amended) A system comprising:  
  
a computing device;  
  
a flash storage system comprising a flash section and at least a portion of a medium ID; and  
  
a controller chip coupled between the computing device and the flash storage system to interface the flash storage system to the computing device, the controller chip comprising an

interface mechanism capable of receiving flash storage systems with controller and controllerless flash storage systems, a detector to determine whether the flash storage system includes a controller for error correction and a flash adapter section which comprises firmware to perform, in an event where the flash storage system does not have a controller for error correction, operations to manage error correction of the flash section, including bad block mapping of the flash section in the flash storage system that is coupled to the flash adapter section.

12. (Original) The system of claim 11, wherein the medium ID contains specifications of the flash storage system.
13. (Amended) The system of claim 12, wherein the flash adapter section further comprises at least another portion of the medium ID.
14. (Original) The system of claim 12, wherein the medium ID comprises a pull-up resistor and a pull-down resistor.

15. (Original) The system of claim 12, wherein the medium ID comprises a voltage divider.
16. (Original) The system of claim 12, wherein the medium ID comprises an EEPROM device to store the specifications of the flash storage system.
- 17-18. Cancel
19. (Amended) The method of claim 7, wherein the flash adapter section further comprises a plurality of interfaces for receiving a plurality of flash storage systems.
20. (Original) The method of claim 7, wherein the bad block mapping includes addressing a new boot sector to allow use of the storage system with a bad boot sector.
21. (Amended) The system of claim 11, wherein the flash adapter section further comprises a plurality of interfaces for receiving a plurality of flash storage systems.

22. (Amended) The [controller chip] system of claim 11, wherein the bad block mapping includes addressing a new boot sector to allow use of the storage system with a bad boot sector.

23-36. Cancel

37. (Added) A flash media interface comprising:  
  
an interface capable of receiving flash media with controller and  
  
controllerless flash media;  
  
means for determining the type of flash medium removably  
  
coupled to the interface thereby determining whether the  
  
flash medium includes a controller for error correction;  
  
means for managing error correction of a flash section of the flash  
  
medium including bad block mapping of the flash section of  
  
the flash medium when the flash media type determined  
  
does have a controller for error correction and thereby does  
  
not itself manage bad block mapping; and  
  
means for providing a second interface to a computing device.

38. Cancel
39. (Added) The flash media interface of claim 37, wherein said means for determining step comprises means for determining a flash medium ID.
40. (Added) The flash media interface of claim 39, wherein said means for determining step comprises means for communicating with said flash medium to determine basic flash medium specifications.
41. (Added) The flash media interface of claim 39, wherein said means for determining step comprises means for detecting voltage levels on predetermined pins of the interface.
42. (Cancelled)
43. (Added) The flash media interface of claim 37, wherein the second interface is selected from a group consisting of USB, IDE, network, or a system bus.
44. (Added) The flash media interface of claim 37, wherein said means for determining comprises a controller IC.

45. (Added) The flash media interface of claim 37, wherein said means for determining comprises firmware.
46. (Added) The flash media interface of claim 37, wherein the computing device comprises driver software for interfacing with flash media.
47. (Added) The flash media interface of claim 37, wherein the second interface to the computing device operates independently of whether the flash media or the flash media interface conducts bad block mapping.
48. (Added) The flash media interface of claim 37, wherein the flash media interface further comprises a flash adapter.
49. (Added) The flash media interface of claim 48, wherein the flash adapter comprises an electro-mechanical interface for differing electro-mechanical flash media formats.
50. (Added) The flash media interface of claim 49, wherein the flash media formats are selected from a group consisting of

CompactFlash, SmartMedia, Secure Digital, MMC, and Memory  
Stick brand flash media formats.

51-64. Cancel

Status of Claims (37 CFR 1.173(c))

1-6	Cancelled
7.	Previously amended
8-10.	Original
11.	Previously amended
12.	Original
13.	Previously amended
14-16.	Original
17-18.	Canceled
19.	Previously amended
20.	Original
21.	Previously amended
22.	Currently amended to remove double brackets
23-36.	Cancelled
37.	Added claim, previously amended
38.	Canceled
39-41.	Previously added claims
42.	Canceled
43-50.	Previously added claims
51-64.	Canceled

**REMARKS**

On March 27, 2013, Hewlett-Packard filed an IPR (IPR2013-00217) with respect to US patent number 7162549. On May 10, 2013, in paper number 8, the Board ordered a stay of the present reissue application. On August 6, 2013, in paper number 31, the Board entered a final written decision in the above-referenced IPR. On September 12, 2014, in paper number 32, the Board lifted the above-referenced stay. On October 6, 2014, MCM filed a notice of appeal to the Federal Circuit of the final written decision. On November 5, 2014, the examiner herein notified applicant that prosecution was reopened and that an appeal brief was due within two months.

Applicant hereby files a § 41.33 Amendment cancelling, without prejudice, all claims that were subject to a rejection or objection. The previous amendment the specification to which the examiner objective is not in compliance with rule 1.173, is, with one exception, identical to the prior moments to specification except for miscellaneous strikethrough's and double-brackets removed and being replaced with single brackets. The exception is the amendment does not include a request to amend paragraph 2 relating to priority.

In addition, a double-brackets in claim 22 has been replaced with a single bracket.

As result of the present amendment, all pending claims stand allowed and the amendments to the specification are now in full compliance with rule 1.173. A supplemental declaration was previously filed on October 29, 2012.

As noted in the advisory action dated May 1, 2013, claims 7-16, 19-22, 37-41 and 43-50 stand allowed. These are the only claims remaining in the present application. Therefore all claims pending stand allowed.

#### STATUS OF CLAIMS

14. The status of the claim(s) is (or will be) as follows:

Claim(s) allowed: 7-16,19-22,37-41 and 43-50.

Claim(s) objected to: 24,38 and 52.

Claim(s) rejected: 17,18,23-27,29-36,51-54 and 56-64.

Claim(s) withdrawn from consideration: .

Applicant respectfully requests reopening of the prosecution for purposes of issuing a notice of allowance of the above-referenced claims.

Respectfully Submitted,

November 14, 2014

/Edward P. Heller III/  
Edward P. Heller, III  
Attorney/Agent for Applicant(s)  
Reg. No. 29,075



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/351,691	01/09/2009	Sreenath Mambakkam	76706-201401-R1	9332
73481	7590	01/12/2015	EXAMINER	
Alliacense Limited LLC			CHEN, ALAN S	
4880 Stevens Creek Boulevard			ART UNIT	
Suite 103			PAPER NUMBER	
San Jose, CA 95129			2129	
			NOTIFICATION DATE	
			DELIVERY MODE	
			01/12/2015	
			ELECTRONIC	

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

emi@alliacense.com  
ip@alliacense.com  
ned@alliacense.com

<b>Office Action Summary</b>	Application No. 12/351,691	Applicant(s) MAMBAKKAM ET AL.	
	Examiner ALAN CHEN	Art Unit 2129	AIA (First Inventor to File) Status No

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 11/14/2014.  
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on \_\_\_\_\_.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on \_\_\_\_\_; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims\*

- 5) ☒ Claim(s) 7-16,19-22,37,39-41 and 43-50 is/are pending in the application.  
5a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 6) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 7) ☒ Claim(s) 7-16,19,21,37,39-41 and 43-50 is/are rejected.
- 8) ☒ Claim(s) 20 and 22 is/are objected to.
- 9) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

\* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see [http://www.uspto.gov/patents/init\\_events/pph/index.jsp](http://www.uspto.gov/patents/init_events/pph/index.jsp) or send an inquiry to [PPHfeedback@uspto.gov](mailto:PPHfeedback@uspto.gov).

### Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

#### Certified copies:

- a) ☐ All    b) ☐ Some\*\*    c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\*\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)  
Paper No(s)/Mail Date 4/4/2013.
- 3) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 4) ☐ Other: \_\_\_\_\_.

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### **DETAILED ACTION**

1. The present application is being examined under the pre-AIA first to invent provisions.
2. Prosecution on the merits of this application is reopened on claims 7-16, 19-22, 37-41 and 43-50. Consideration is made in light of the final written decision by the PTAB on 8/6/2014 for US Pat. No. 7,162,549, in which this instant application is a reissue thereof, and the Information Disclosure Statements submitted on the 4/4/2013.

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 7-9, 11-13, 16, 19, 21, 37, 39-41 and 43-50 are rejected under 35 USC 103(a) as being unpatentable over US Pat. No. 6,199,122 to Kobayashi in view of International Application WO 98/03915 to Kikuchi (*cited in the IDS submitted on 4/4/2013*).
5. Claims 10, 14 and 15 are rejected under 35 USC 103(a) as being unpatentable over US Pat. No. 6,199,122 to Kobayashi in view of International Application WO 98/03915 to Kikuchi (*cited in the IDS submitted on 4/4/2013*) in further view of US Pat. No. 6,121,087 to Mann et al. (*hereinafter Mann*).

### **Independent Claims**

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6. Per claims 7, Kobayashi discloses a method comprising: using a controller (*fig. 11, item 12 shows various functional blocks, specifically items 122, 123, 124 and 134 all of which is construed as a controller...that allow control of commands and data between a host computer, item 111 and external flash memory, items 13*) to interface (*fig. 11, item 125, an interface*) a flash storage system with or without a controller (*fig. 2, item 13 is a flash storage system comprising flash memory without an ATA controller; fig. 10, item 13 is a flash storage system comprising flash memory with an ATA controller*) to a computing device (*fig. 11, item 111*), the controller comprising a flash adapter section (*fig. 11, items 122 and 123; col. 6, lns 23-43 and col. 8, lns 14-38, ROM contains operational instruction that adapts commands and data from computer, e.g., USB, to formats suitable to external memory*), wherein the flash storage system comprises a flash section (*fig. 2, item 131 and fig. 10, item 131*) and at least a medium ID (*col. 7, lns 25-32, CIS data; col. 7, ln 65-col 8, ln 38, external storage has specifications such as device type, product ID, etc., all of which can be construed as a medium ID; col. 11, lns 3-7, another specification obtained from fixed area in memory card is capacity, among other things*); determining whether the flash storage system (*item 13*) includes a controller (*fig. 11, items 133 and 134; col 12, lns 59+, the type of memory card can be determined, specifically whether the memory card has a controller, such as the one shown in fig. 10, item 13 or whether the memory card does not have a controller, such as the one shown in fig. 2, item 13*); and in an event where the flash storage system does not have a controller, using firmware in the flash adapter section to perform operations to manage the flash section (*fig. 1 shows effectively what the functional*

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*embodiment of fig. 11 is when there is a determination that the external memory has no controller; col. 6, lns 23-43...ROM, item 123, allows commands to be translated between computer and flash memory, e.g., USB and ATA).*

Per claim 11, Kobayashi discloses a system (*fig. 11*) comprising: a computing device (*fig. 11, item 111*); a flash storage system (*fig. 11, items 13*) comprising a flash section (*fig. 2, item 131 and fig. 10, item 131*) and at least a portion of a medium ID (*col. 7, lns 25-32, CIS data; col. 7, ln 65-col 8, ln 38, external storage has specifications such as device type, product ID, etc., all of which can be construed as a medium ID; col. 11, lns 3-7, another specification obtained from fixed area in memory card is capacity, among other things*); and a controller (*fig. 11, item 12 shows various functional blocks, specifically items 122, 123, 124 and 134 all of which is construed as a controller...that allow control of commands and data between a host computer, item 111 and external flash memory, items 13*) coupled between the computing device and the flash storage system to interface the flash storage system to the computing device (*fig. 11*), the controller comprising an interface mechanism (*fig. 11, item 125, an interface*) capable of receiving flash storage systems with controller and controllerless flash storage systems (*fig. 2, item 13 is a flash storage system comprising flash memory without an ATA controller; fig. 10, item 13 is a flash storage system comprising flash memory with an ATA controller*), a detector to determine whether the flash storage system includes a controller (*fig. 11, items 133 and 134; col 12, lns 59+, the type of memory card can be determined, specifically whether the memory card has a controller, such as the one shown in fig. 10, item 13 or whether the memory card does not have a controller, such*

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*as the one shown in fig. 2, item 13) and a flash adapter section which comprises firmware to perform, in an event where the flash storage system does not have a controller for error correction, operations to manage the flash section (fig. 11, items 122 and 123; col. 6, lns 23-43 and col. 8, lns 14-38, ROM contains operational instruction that adapts commands and data from computer, e.g., USB, to formats suitable to external memory).*

Per claim 37, a flash media interface (*fig. 11*) comprising: an interface (*fig. 11, item 125, an interface*) of receiving flash media with controller and controllerless flash media (*fig. 2, item 13 is a flash storage system comprising flash memory without an ATA controller; fig. 10, item 13 is a flash storage system comprising flash memory with an ATA controller*); means for determining the type of flash medium removably coupled to the interface thereby determining whether the flash medium includes a controller (*fig. 11, items 133 and 134; col 12, lns 59+, the type of memory card can be determined, specifically whether the memory card has a controller, such as the one shown in fig. 10, item 13 or whether the memory card does not have a controller, such as the one shown in fig. 2, item 13*); means for managing a flash section of the flash medium when the flash media type determined does have a controller (*fig. 11, items 122 and 123; col. 6, lns 23-43 and col. 8, lns 14-38, ROM contains operational instruction that adapts commands and data from computer, e.g., USB, to formats suitable to external memory*); and means for providing a second interface to a computing device (*fig. 11, item 121*).

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As related to claims 7, 11 and 37, Kobayashi further discloses the ability to check for errors in the flash memory such as bad blocks, by the flash adapter section (*col. 11, lns 25-45, errors in memory can be detected*).

Kobayashi does not disclose the controller (*fig. 11, item 12*) being on single integrated chip. Kobayashi also does not expressly state error correction being performed or error correction including mapping bad blocks in the flash memory.

Kikuchi teaches a flash memory reader (*figs. 15A and 15B*) being able to handle flash memory cards with or without controllers. Kikuchi teaches the controller on the flash memory reader being a single integrated chip (*fig. 2; pg 9, lns 10-15*). Kikuchi further teaches error correction being performed by the controller to include mapping of bad blocks in flash memory (*fig. 2, item 32; pg. 13, lns 17-19*).

Kobayashi and Kikuchi are analogous art because both describe ATA controllers that work with controller and controllerless flash memory cards. Kobayashi invention lends itself to error correction when Kobayashi expressly states checking for errors (*col. 11, lns 25-45*).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to have the controller in Kobayashi's invention (*fig. 11, item 12*) integrated on a single chip as shown by Kikuchi, rather than spread out among multiple chips with various electrical elements and interconnects linking them on a circuit board. The motivation for doing so would have been the various well-known advantages that comes with integration including reduced power consumption, smaller form factor allowing for more portability, reduced material and manufacturing costs, to name a few.

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Further, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to include error correction, specifically bad block mapping as shown by Kikuchi into Kobayashi's controller (*fig. 11, item 12*). The motivation for doing so would have been that reparable errors detected by Kobayashi (*col. 11, Ins 25-45*), such as the inability to write to a bad block, can be mitigated by rerouting the write command to another usable block. Rather than render an entire flash memory unusable due to a very small percentage of bad blocks in the overall usable flash memory, correcting for bad blocks will allow preservation of the flash memory and increasing reliability.

### **Dependent Claims**

6. Per claims 8,12,16, 39 and 40, Kobayashi combined with Kikuchi discloses claims 7,11 and 37 Kobayashi further disclosing storing specifications of the flash storage system in the medium ID (*col. 7, Ins 25-32, CIS data; col. 7, In 65-col 8, In 38, external storage has specifications such as device type, product ID, etc., all of which can be construed as a medium ID; col. 11, Ins 3-7, another specification obtained from fixed area in memory card is capacity, among other things*).

7. Per claim 9, Kobayashi combined with Kikuchi discloses claim 7, Kobayashi discloses storing a capacity parameter of the memory card in a fixed area within the memory card's flash memory (*col. 11, Ins 3-7 of Kobayashi, specification obtained from fixed area in memory card is capacity*). Kikuchi teaches substituting bad blocks that have an error or have failed (*pg. 13, Ins 17-21 of Kobayashi*). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to update at

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least the storage capacity parameter in Kobayashi to reflect the total storage capacity to account for bad blocks. The motivation for doing so is to accurately present to the user of the memory card the exact usable storage capacity in order for the user to know how much data he/she can store on the card and whether another memory card with a larger storage capacity is needed.

8. Per claims 10, 14 and 15, Kobayashi combined with Kikuchi discloses claims 7 and 11. Kobayashi does not disclose how the flash memory is designed at a circuit level. Mann discloses CMOS ROM cells used to implement flash memory (*col. 1, Ins 37-col. 3, Ins 6*) having several advantages over other flash memory circuit designs, including faster switching for writing to the flash memory, reduced manufacturing costs. It is well known that CMOS technology uses pull up and pull down transistors and other fundamental circuit building blocks such as voltage dividers to represent digital bits. At the time of the invention, it would have been obvious to implement the flash memory of Kobayashi in combination with Kikuchi, using CMOS suggested by Mann et al., in order to gain the various aforementioned advantages gained using CMOS circuit design.

9. Per claims 13, Kobayashi combined with Kikuchi discloses claim 12, Kobayashi further disclosing the flash adapter section comprises at least another portion of the medium ID (*col. 7, Ins 25-32, CIS data; col. 7, In 65-col 8, In 38, external storage has specifications such as device type, product ID, etc., all of which can be construed as a medium ID*).

10. Per claims 19 and 21, Kobayashi combined with Kikuchi discloses claims 7 and 11, Kobayashi further disclosing the flash adapter section further comprises a plurality

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of interfaces for receiving a plurality of flash storage systems (*fig. 12, items 125A and 125B*).

11. Per claim 41, Kobayashi combined with Kikuchi discloses claims 39, Kobayashi further discloses the flash memory card having physical pins (*figs. 2 and 10, item 132*) with corresponding pins on interface (*fig. 11, item 125*), inherently having varying voltage levels that are sensed/detected for communication.

12. Per claim 43, Kobayashi combined with Kikuchi discloses claims 37, Kobayashi further disclosing the second interface can be USB (*col. 5, lns 59-65*).

13. Per claim 44, Kobayashi combined with Kikuchi discloses claims 37, Kikuchi teaching the controller being one integrated circuit (*fig. 2; pg 9, lns 10-15*).

14. Per claim 45, Kobayashi combined with Kikuchi discloses claim 37, Kobayashi further disclosing the means for determining comprises firmware (*fig. 11, items 122 and 123; col. 6, lns 23-43 and col. 8, lns 14-38, ROM contains operational instruction that adapts commands and data from computer, e.g., USB, to formats suitable to external memory*).

15. Per claim 46, Kobayashi combined with Kikuchi discloses claim 37, Kobayashi further disclosing the computing device comprises driver software for interfacing with flash media (*col. 6, lns 54-57, computer having a dedicated device driver*).

16. Per claim 47, Kobayashi combined with Kikuchi discloses claim 37, Kobayashi further disclosing the second interface to the computing device operates independently of whether the flash memory card has a controller or is controllerless (*figs. 12 and 13*).

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17. Per claims 48 and 49, Kobayashi combined with Kikuchi discloses claim 37, Kobayashi further disclosing the flash media interface further comprises a flash adapter (*figs. 11-13, item 125*) adaptable to various electro-mechanical flash media formats (*flash memory cards having a controller may have different electro-mechanical formats and those that are controllerless may have different electro-mechanical formats*).

18. Per claim 50, Kobayashi combined with Kikuchi discloses claim 49. Kikuchi further teaches the ability to adapt to the SmartMedia format as well as various other formats (*pg. 33, Ins 2-7*). At the time of the invention it would have been obvious for the controller and controllerless flash memory cards that Kobayashi can accommodate to be one of the popular and more widely used formats such as SmartMedia, CompactFlash, Secure Digital, etc. The motivation for using these formats is the large market share that Kobayashi's invention can be applied to and the convenience that follows for the wide user base that uses these popular formats.

***Allowable Subject Matter***

19. Claims 20 and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Contact Information***

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ALAN CHEN whose telephone number is (571) 272-4143. The examiner can normally be reached on M-F 9-5.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey A. Gaffin can be reached on (571) 272-4146. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ALAN CHEN/  
Primary Examiner, Art Unit 2129  
12/30/2014

<b>Notice of References Cited</b>	Application/Control No. 12/351,691	Applicant(s)/Patent Under Reexamination MAMBAKKAM ET AL.	
	Examiner ALAN CHEN	Art Unit 2129	Page 1 of 1

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,121,087	09-2000	Mann et al.	438/258
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Doc code: IDS

PTO/SB/08a (01-10)

Doc description: Information Disclosure Statement (IDS) Filed

Approved for use through 07/31/2012. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> ( Not for submission under 37 CFR 1.99)	Application Number		12351691	
	Filing Date		2009-01-09	
	First Named Inventor	Mambakkam, Sreenath		
	Art Unit	2129		
	Examiner Name	Chen, Alan S.		
	Attorney Docket Number	76706-201401-R1		

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	1	<del>5823845</del> 9803915	WO		1998-01-29	Tokyo Electron Limited		<input type="checkbox"/>

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**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**  
( Not for submission under 37 CFR 1.99)

Application Number	12351691
Filing Date	2009-01-09
First Named Inventor	Mambakkam, Sreenath
Art Unit	2129
Examiner Name	Chen, Alan S.
Attorney Docket Number	76706-201401-R1

1	Petition for Inter Partes Review for Patent No. 7,162,549, Hewlett-Packard Company (Petitioner) v. MCM Portfolio LLC (Patent Owner), Filed 3/27/2013.	<input type="checkbox"/>
2	Notice of Filing Date Accorded to Petition and Time for Filing Patent Owner Preliminary Response for Inter Partes Review for Patent No. 7,162,549, Hewlett-Packard Company (Petitioner) v. MCM Portfolio LLC (Patent Owner), Mailed 3/29/2013.	<input type="checkbox"/>
3	Petitioner Power of Attorney for Inter Partes Review for Patent No. 7,162,549, Hewlett-Packard Company (Petitioner) v. MCM Portfolio LLC (Patent Owner), Dated 3/27/2013.	<input type="checkbox"/>
4	Chee-Kong AwYong, "An Integrated Control System Design of Portable Computer Storage Peripherals", June 2000.	<input checked="" type="checkbox"/>
5	Samsung K9D1208V0M Datasheet, Samsung Electronics.	<input type="checkbox"/>
6	Declaration of Sanjay Banerjee, PH. D., Dated 3/26/2013.	<input type="checkbox"/>
7	Witness Statement of Dr. Robert Ellett Regarding Public Accessibility of Certain References, Inv. No. 337-TA-841, Dated 12/4/2012.	<input type="checkbox"/>
8	Declaration of Dr. Robert Ellett Regarding Public Accessibility of Certain References, Inv. No. 337-TA-753, Dated 10/18/2012.	<input type="checkbox"/>
9	Chinese MARC Record.	<input checked="" type="checkbox"/>
10	Back Cover of AwYong Thesis.	<input checked="" type="checkbox"/>
11	AwYong Thesis Certificate of Publication, Dated 12/22/2000.	<input checked="" type="checkbox"/>

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**  
( Not for submission under 37 CFR 1.99)

Application Number		12351691
Filing Date		2009-01-09
First Named Inventor	Mambakkam, Sreenath	
Art Unit	2129	
Examiner Name	Chen, Alan S.	
Attorney Docket Number	76706-201401-R1	

12	US Patent No. 7,162,549 Patent Prosecution File History.	<input type="checkbox"/>
13	Affidavit of Christopher Butler, Dated 3/21/2013.	<input type="checkbox"/>
14	"CF+ and CompactFlash Specification Rev. 1.4", CompactFlash Association, 1999.	<input type="checkbox"/>
15	"MultiMediaCard Product Manual Rev. 2", SanDisk Corporation, 2000.	<input type="checkbox"/>
16	"SD memory card specifications, part 1, physical layer specification Ver. 1.00", SD Group, March 2000.	<input type="checkbox"/>
17	"The Multi Media Card System Specification Ver. 2.11", MMCA Technical Committee, June 1999.	<input type="checkbox"/>
18	"MemoryStick Standard Format Specifications Ver. 1.2", Sony Corporation, July 1999.	<input type="checkbox"/>
19	"SmartMedia Software Algorithm Guidelines Ver. 1.00", SSFDC Forum Technical Committee, 5/19/2000.	<input type="checkbox"/>
20	"SmartMedia ECC Reference Manual Ver. 2.1", Toshiba Corporation, 9/15/1999.	<input type="checkbox"/>
21	"SMIL (SmartMedia Interface Library) Hardware Edition Version 1.00", Toshiba Corporation., July 1, 2000.	<input type="checkbox"/>
22	"SmartMedia Electrical Specifications Web-Online V. 1.00", SSFDC Forum Technical Committee, 5/19/1999.	<input type="checkbox"/>

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**  
( Not for submission under 37 CFR 1.99)

Application Number	12351691
Filing Date	2009-01-09
First Named Inventor	Mambakkam, Sreenath
Art Unit	2129
Examiner Name	Chen, Alan S.
Attorney Docket Number	76706-201401-R1

23	CV of Dr. Sanjay Kumar Banerjee.	<input type="checkbox"/>
24	Affidavit of Abraham Holczer.	<input type="checkbox"/>
25	Information Disclosure Statements from US Patent Application No.12/351,691. (as of 03-26-13)	<input type="checkbox"/>
26	Inv. No. 337-TA-841, Complaint Technology Properties Limited, LLC's Proposed Claim Constructions, Dated 10/5/2012.	<input type="checkbox"/>
27	Inv. No. 337-TA-841, Order Construing the Terms of the Asserted Claims of the Patents at Issue, Dated 10/4/2012.	<input type="checkbox"/>
28	Inv. No. 337-TA-841, Complainant Technology Properties Limited's Post-Hearing Brief (Redacted), Pages 262-264, 291-293, Dated 1/29/2013.	<input type="checkbox"/>
29	Inv. No. 337-TA-841, Complainant Technology Properties Limited LLC's Post-Hearing Reply Brief (Redacted), Pages 83-86, 131-133, Dated 2/11/2013.	<input type="checkbox"/>
30	Inv. No. 337-TA-841, Testimony of Stanley Moyer, Executive Director of the SD Association, Page 1297-1329, Dated 1/9/2013.	<input type="checkbox"/>
31	Inv. No. 337-TA-841, ITC Investigation Open Session Trial Transcript, Dated 1/4/2013-1/10/2013.	<input type="checkbox"/>

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**EXAMINER SIGNATURE**

Examiner Signature	/Alan Chen/	Date Considered	12/29/2014
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\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<b><i>Search Notes</i></b>	<b>Application/Control No.</b>	<b>Applicant(s)/Patent Under Reexamination</b>
	<b>Examiner</b>	<b>Art Unit</b>

<b>CPC- SEARCHED</b>		
<b>Symbol</b>	<b>Date</b>	<b>Examiner</b>

<b>CPC COMBINATION SETS - SEARCHED</b>		
<b>Symbol</b>	<b>Date</b>	<b>Examiner</b>

<b>US CLASSIFICATION SEARCHED</b>			
<b>Class</b>	<b>Subclass</b>	<b>Date</b>	<b>Examiner</b>

<b>SEARCH NOTES</b>		
<b>Search Notes</b>	<b>Date</b>	<b>Examiner</b>

<b>INTERFERENCE SEARCH</b>			
<b>US Class/ CPC Symbol</b>	<b>US Subclass / CPC Group</b>	<b>Date</b>	<b>Examiner</b>

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No. 15-1091

United States Court of Appeals  
for the Federal Circuit

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MCM PORTFOLIO LLC,  
APPELLANT,

v.

HEWLETT-PACKARD COMPANY,  
APPELLEE.

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**PROOF OF SERVICE**

I, Emi Rhodes, being duly sworn according to law and being over the age of 18, upon my oath depose and say that on **February 10, 2015**, Edward Heller, counsel for appellant, authorized me to electronically file the foregoing **MOTION TO STAY REISSUE** with the Clerk of Court using the CM/ECF System, which will serve via e-mail notice of such filing to counsel for Appellee pursuant to Fed. R. App. P. 25 and Fed. Cir. R. 25(a) and 25 (b).

/s/ Emi Rhodes

Emi Rhodes